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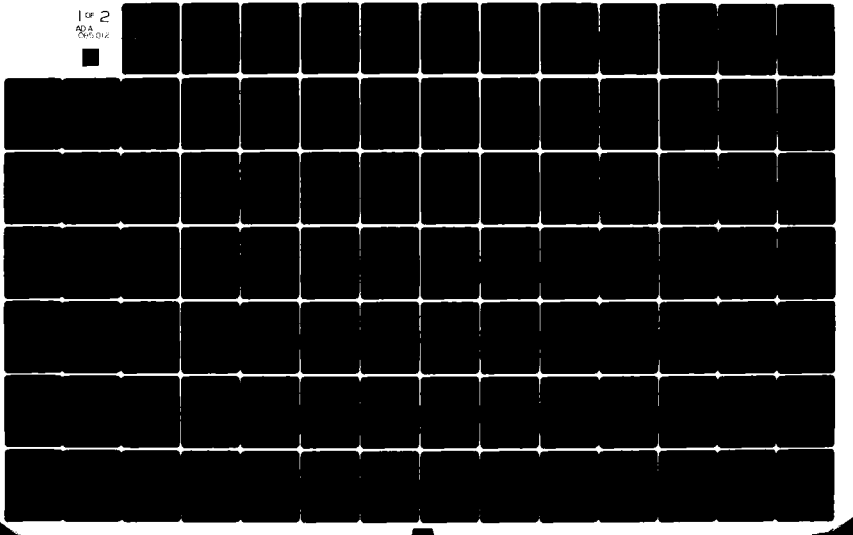

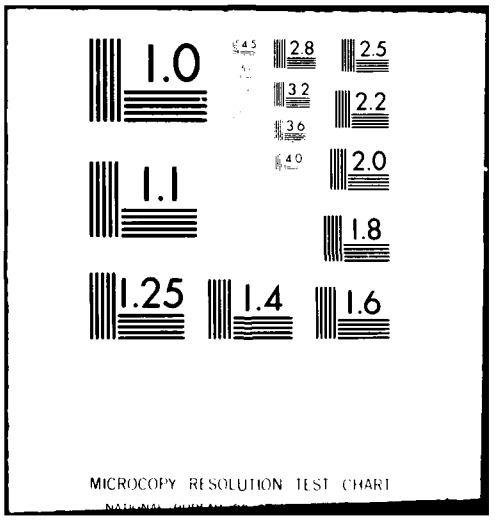
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PHASE I COMPLETION REPORT
TOTAL DOSE HARDNESS ASSURANCE

Volume I: Identification of Techniques

BDM Corporation
Albuquerque, NM 87106

February 1980

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Final Report

Approved for public release; distribution unlimited

This research was sponsored by the Defense Nuclear Agency under Subtask Z99QAXTD072, Work Unit 14, Hardness Assurance Techniques for LSI Devices.

Prepared for

Director
DEFENSE NUCLEAR AGENCY
Washington, DC 20305

AIR FORCE WEAPONS LABORATORY
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AFWL-TR-79-53, Vol. I

This final report was prepared by BDM Corporation, Albuquerque, New Mexico, under Contract F29601-78-C-0022, Job Order 88091133 with the Air Force Weapons Laboratory, Kirtland Air Force Base, New Mexico. Mr. Roe J. Maier (NTMP) was the Laboratory Project Officer-in-Charge.

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This technical report has been reviewed and is approved for publication.

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This report covers the first phase of a three phase program to develop hardness assurance techniques for the total ionizing radiation dose environment for bipolar and MOS semiconductor devices. Phase I consists of identifying and verifying potentially useful techniques. The report is presented in two volumes. Volume one discusses all of the potential hardness assurance techniques that were identified and whether or not they are sufficiently verified in previous studies. In addition, new techniques are proposed based on models of radiation-induced hole trapping and interface state generation. (over)

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Each technique identified or proposed is discussed in terms of its implementation, cost effectiveness, and acceptability. Recommendations are made for each technique to: a. reject for this program, b. verify its usefulness with further testing or, c. accept as useful and include in the evaluation phase. The techniques investigated fall into into five major categories: 1. preirradiation device electrical tests, 2. preirradiation tests on special test devices or wafers, 3. process or design controls, 4. radiation simulation tests, and 5. radiation tests. Over 20 techniques were identified and 9 were selected for further studies.

Volume II is a summary of the test results of the verification tests performed on commercial semiconductor devices. These verification tests were performed either to supplement the limited available data for a potentially useful technique or to generate original data on previously unexamined techniques. The correlation coefficient was determined between the screening parameter and the total dose induced change in device electrical parameters on groups of 5-25 devices of a given type. No high degree of correlation was observed for any of the techniques investigated with the exception of irradiate and anneal on MOS devices.

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PREFACE

This report was prepared by the BDM Corporation, 2600 Yale Blvd., S.E., Albuquerque, NM 87106 for the Air Force Weapons Lab under Contract F29601-78-C-0022. The project officer for the Air Force was Mr. Roe J. Maier. The program manager and principal investigator for BDM was Mr. Ronald L. Pease.

This report covers the first phase of a three phase program to develop Total Dose Hardness Assurance Techniques for MOS and bipolar semiconductor devices. The first phase involves identification and verification of techniques. In the process of identifying potential hardness assurance techniques, many discussions were held with other investigators. The authors wish to acknowledge many useful discussions with the project officer, Mr. Roe Maier, Dr. Gary Derbenwick of Sandia Labs, and Dr. Kenneth Galloway of the National Bureau of Standards.

Volume I of this report, Identification of Techniques, was written by Mr. Ronald Pease and Volume II, Verification Test Results, was written primarily by Mr. Phil Young.

SECTION I
PROGRAM OBJECTIVES

The objective of the total dose ionizing radiation hardness assurance program is to develop techniques applicable for MOS and bipolar technologies to assure that devices going into military systems meet performance requirements at specified levels of ionizing radiation. This objective applies either to single devices or to a production lot of devices. When applied to single devices, the technique involves a screening process that is performed on every device to assure that it will pass the requirements. The desired screening method would involve a nondestructive electrical or mechanical test performed on an unirradiated or unstressed part that could be used to predict the amount of degradation the part would see at a certain total dose level. In the absence of a preirradiation screen, the only 100 percent test would have to involve stressing the part to obtain the desired effect (by irradiation or other means), measuring the amount of degradation and then annealing out the damage. This method works only if the degradation is quantitatively repeatable. In lieu of a 100 percent screen, the objective can be met on a statistical basis by characterizing a specified lot of devices by sample testing. The definition of "lot" and the number of samples requiring testing are determined by the confidence required and the number of allowed failures (lot tolerance percent defective). Sample testing could be applied to either preirradiation (destructive or nondestructive) or radiation tests.

Whether one chooses a 100 percent screen or a sample test is determined primarily by the criticality of the part and the system requirements. In satellite programs, failure of a single critical part can abort the mission. Therefore, screening is essential if the distribution of total dose failure levels is even close to the specification limit. On the other hand, in a missile system, failure of a part could mean that a particular missile (out of several fired) cannot carry out its mission, but more often, the critical part failure will mean that the probability of a hit is degraded. Thus, a few part failures can occur without

total mission failure. This program is directed at finding practical and cost-effective solutions to both problems.

In order to meet the objective, the program is divided into three phases. The first phase involves identifying potential total dose hardness assurance techniques and verifying those techniques for which there are insufficient data to determine their effectiveness and practicality. The second phase involves a detailed evaluation in a production environment of all the techniques determined to be effective and practical. The third phase involves documentation of techniques evaluated in phase II and development of detailed test procedures for implementing the techniques.

The specific objective of the phase I identification effort is to identify, by whatever means possible, all hardness assurance techniques which could potentially meet the program objective. Once the techniques have been identified, they are analyzed in terms of their effectiveness (ability to predict total dose response) and practicality (how easily they could be implemented on a production line). If there are insufficient data to determine the effectiveness and practicality of the method, a verification test is required before the technique is accepted or rejected for evaluation.

The specific objective of the phase I verification effort is to subject each technique to tests and analyses sufficient to determine its effectiveness and practicality.

SECTION II
PHASE I APPROACH

1. IDENTIFICATION

The identification of potential total dose hardness assurance techniques involved reviewing the literature pertinent to the subject and attempting to conceive of new approaches. The specific approaches taken in this program were:

(1) Perform professional literature searches.

(2) Perform literature searches using reference lists and bibliographies -- especially from review papers.

(3) Talk to other investigators in the area of total dose effects and hardening.

(4) Identify or conceive of techniques based on models used to describe the basic mechanisms.

a. Professional Literature Searches

Two professional literature searches were used in this program. The first was performed by the University of New Mexico Technical Applications Center (TAC). This search included only unclassified articles written in English or translated into English. The available journals included all IEEE publications.

The search produced an unedited total of 510 articles covering radiation effects, modeling, and test techniques for surface effects. After a careful review of the total list, 30 articles were identified (in addition to the articles published in IEEE Transactions on Nuclear Science) as being useful to this program.

A second literature search was conducted by the Defense Documentation Center which included both an NTIS open literature search and a Government documents search. This unclassified search, including documents dated within the last 10 years, produced an unedited list of 342 articles. Of these, 35 were found to be relevant to this program.

b. Literature Search From Reference Lists and Bibliographies

The difficulty in generating a comprehensive list of relevant articles from a professional service computer file lies mainly in identifying the appropriate key words. Oftentimes, the list of key words associated with an article are not sufficient. Therefore, many articles which are relevant are not identified in the computer search. A much more efficient and pragmatic way of identifying relevant literature is to utilize the efforts of other investigators. This was done by reviewing the list of references and bibliographies taken from "review" papers (e.g., invited papers on total dose effects presented at the IEEE Annual Nuclear and Space Radiation Effects Conference) and other articles on total dose hardening, hardness assurance, and basic mechanisms. By starting with a few recent papers having extensive reference lists one can quickly identify most of the relevant material.

c. Personal Contact With Other Investigators

Although an extensive literature base is essential for identifying potential techniques, it is not sufficient. Many hardness assurance techniques which may have some merit do not appear in the literature for many reasons. If results are negative, they are generally not published, unless required by contract. However, even though a technique produced negative results for a specific device type or application, it may be useful for a different technology or application. Other techniques which could prove useful may have been tried but were not published due to programs being cut off or researchers changing jobs and not continuing the investigation. Whatever the reason, there are techniques and methods which have been conceived and investigated but never reported. In addition, many investigators have tried techniques which have been reported in the literature and received different results. These data do not always appear in the literature.

Therefore, in order to derive a more complete set of data on a particular technique, or to identify additional techniques, it is necessary to talk with investigators active in total dose effects programs.

Contact with a number of investigators was accomplished by telephone and by holding a workshop on Total Dose Hardness Assurance. The workshop, to be discussed in a later section, was held at BDM in conjunction with the annual IEEE Conference on Nuclear and Space Radiation Effects. Over 30 people active in total dose radiation effects were present.

d. Techniques Conceived From Consideration of Models of Total Dose Mechanisms

The final approach to identifying total dose hardness assurance techniques was to consider models proposed to explain the basic mechanisms of total dose degradation. If one accepts certain models to explain hole trapping, tests should be available to measure the process-induced hole traps or defects which give rise to hole traps upon irradiation.

In a similar manner, tests should be available to verify different models of defects which give rise to radiation-induced changes in interface state density. Consideration of these models not only leads to newly conceived hardness assurance techniques, but provides rationale for techniques which have been tried in the past.

2. FILTERING PROCESS FOR TECHNIQUES IDENTIFIED AS POTENTIALLY USEFUL

The objective of the filtering process is to determine the effectiveness and practicality of the potential technique to determine if:

(1) The technique should be rejected.

(2) The technique requires verification because of insufficient data.

(3) The technique is accepted as effective and practical and should be evaluated in a production environment.

A flow diagram of the filtering process is given in Figure 1.

The criterion for determining whether or not a technique is effective is whether or not it can predict the total dose response of either individual devices or a process lot with reasonably high confidence. The decision as to whether or not the technique meets this criterion must be based on actual data. In addition to actual data, the effectiveness must

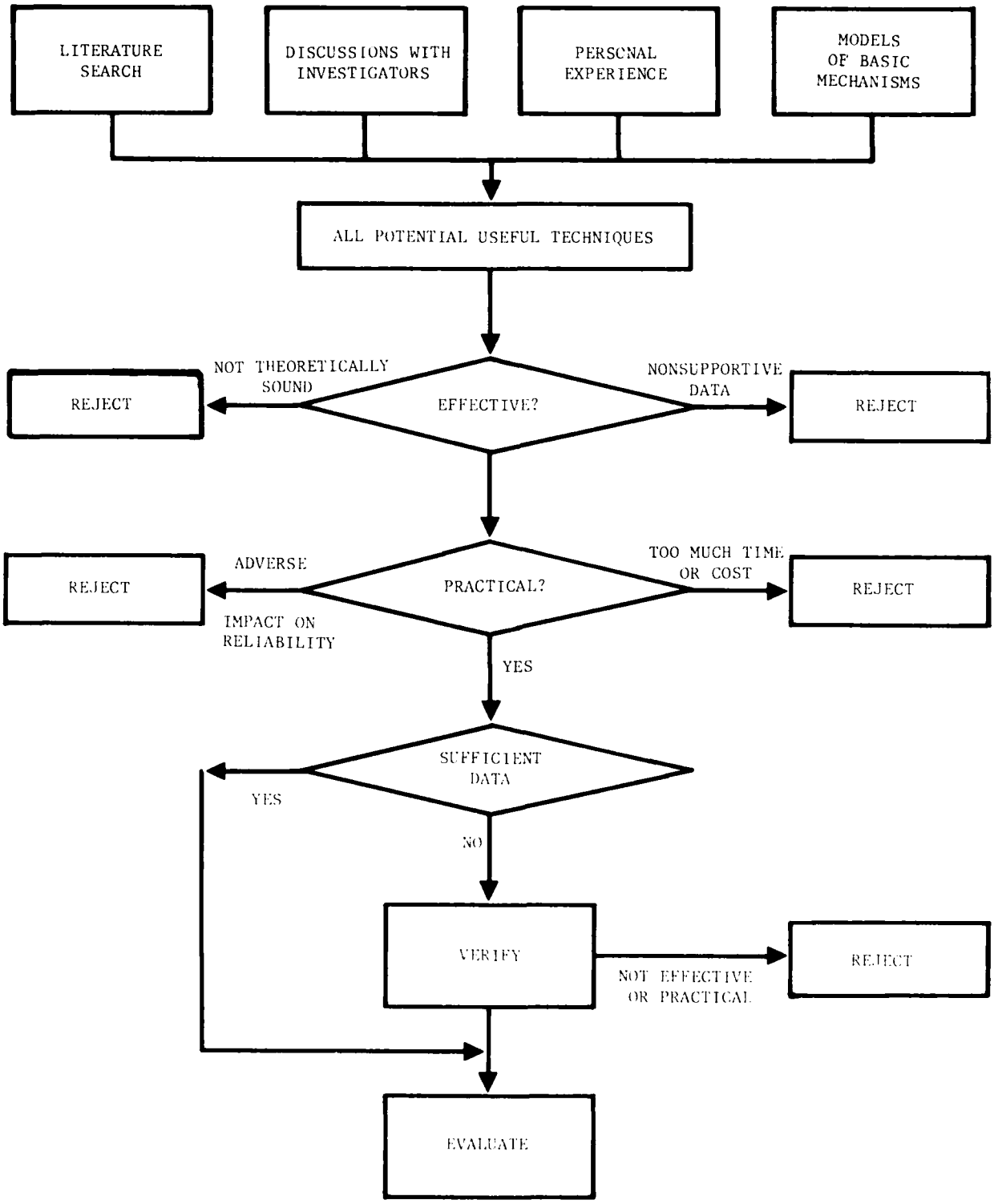

Figure 1. Filtering For Potentially Useful Screens

also be determined from the physical rationale for the technique. If there are no theoretical grounds for accepting the technique as a valid approach, and correlation is merely coincidental, then the technique may be rejected as ineffectual even though positive data exist for a particular device. Therefore, to be considered effective, a technique must have a sound rationale as well as supportive data. If either is lacking, the technique must be rejected or subjected to additional verification tests and analyses.

Even though a technique is shown to be effective, it must also be considered practical before it will be evaluated in a production environment. The criteria for practicality include the following considerations:

(1) Is the test time, hence labor costs, excessive?

(2) Will the technique adversely affect the reliability of the part if it is to be applied as a 100 percent screen?

(3) Will the capital equipment requirements be excessive?

(4) Will the technique require special test devices which are difficult to incorporate on a wafer?

(5) Does the technique require special equipment which cannot easily be obtained?

(6) Is the sensitivity of the measurement too great for production handling?

Although the list is not exhaustive, factors such as these must be considered if the the technique is to be implemented on production parts without prohibitive cost and still be acceptable to vendors, users, and program offices.

If there is sufficient information available to determine the effectiveness and practicality of the technique, a decision is made whether to reject or evaluate the technique. If insufficient information exists to make a reasonable decision, the technique must be verified by further tests and analyses. The verification task is not intended to be as extensive as the evaluation phase. Verification testing is performed only to determine the effectiveness and practicality of the screen.

3. VERIFICATION

The intent of verification was to perform experimental tests and analyses on those techniques whose usefulness was in question in order to make a decision as to whether or not to expend the necessary manpower for evaluation of the technique in a production environment. Although this appeared to be a reasonable approach, it quickly became difficult to implement. Most of the techniques which were identified as potentially effective and practical had not been subjected to experimental verification by other investigators. Other techniques which had been experimentally pursued by more than one investigator were in question because of conflicting results. Therefore, nearly all techniques which were not rejected outright required extensive verification testing. Only two or three techniques were accepted as having been sufficiently verified in previous studies.

Several of the techniques which required verification involved the use of special test structures or test wafers. Since no provisions were made in the program plan for specially fabricated devices or wafers, these techniques were not verified in phase I. Phase II (evaluation) was restructured to allow verification of all techniques involving special test devices and wafers. Therefore, phase I verification was limited to those techniques which could be experimentally investigated using commercially available devices.

The approach to be discussed in this report for verification was that taken for phase I verification using commercially available devices. The primary portion of verification was experimental data taken on actual devices to determine the degree of correlation between the prediction parameter and the radiation response of the device. These experimental data were supplemented by physical arguments to support the technique based on a model of the basic mechanisms and by an assessment of the practicality of the technique for production testing.

Several experimental approaches are possible for verifying a correlation between a prediction parameter and the actual radiation response of a

device. If the prediction parameter is a nondestructive preirradiation electrical measurement, then the approach is very simple. A sample of devices is characterized for the prediction parameter, irradiated, and then analyzed for the correlation between the parameter and the radiation induced change in the device critical electrical parameters. However, if the hardness assurance technique involves a temperature or electrical stress test as a prediction of radiation response, the verification is not straightforward. Possible approaches are:

(1) Obtain samples of many different types of devices. Stress half the samples of each type and record the average change. Irradiate the other half and record the change. Then compare the average stress-induced change to the average radiation-induced change. If a high degree of correlation exists, the technique can be used to determine which device types are harder.

(2) Obtain large samples of one or more device types. Stress the samples to produce a small but easily measureable change. Then irradiate the same samples to produce an additional small but easily measureable change. Compare the stress induced and radiation induced changes on the same devices. A high degree of correlation indicates that the stress adequately simulates the radiation.

(3) Obtain a large sample of like pairs of devices. These should be pairs that are located side by side on a wafer. This can sometimes be accomplished by buying closely matched dual devices. For instance, some dual transistors are side-by-side devices whose chips are still connected. Also, some dual or quad linear circuits are all contained in a single chip. If these devices can be obtained, half of the pair can be stressed, leaving the other half undisturbed. The package can then be irradiated and the unstressed half characterized for radiation response. The stress induced change on one half and the radiation induced change on the other half can be compared. Good correlation would indicate that the stress is a good simulation of the radiation.

(4) Obtain a large sample of one or more device types. Stress the devices and measure the change in electrical parameters from the stress. Then anneal the damage out under elevated temperature to restore the device to within a specified percentage of its initial value. Irradiate the same devices and determine the radiation induced change in critical electrical parameters. Compare the stress induced changes to the radiation-induced changes.

The first approach requires the testing of many different device types and does not provide assurance that within a given type, the technique is valid. It is used in those cases where nominal hardness is more important than the response of individual devices. The second approach assumes that the response curves of all devices of a given type are proportional over the total dose range used. This is not a valid assumption for many device types, especially linear circuits. The third approach is valid except for "maverick" devices. Also, it is very limited since it can be used only on a few device types.

The approach used in this program for verifying techniques involving "destructive" tests, such as stress tests, was the fourth approach. The major consideration in this approach is how well the device can be restored to its initial condition by the thermal annealing. The assumption was made that the stressing merely resulted in filling hole traps and creating interface states without forming new hole traps or causing irreversible chemical changes at the interface. The validation of this assumption would require extensive, well controlled testing which was not intended for this program.

The approach to verifying the practicality of the various techniques was to consider possible ways of implementation in a production environment and discussing the time, equipment, cost, and processing implications with semiconductor vendors. The determination of practicality is somewhat subjective since the major factor is usually cost. The cost factor is controlled by the particular user's budget and his commitment to total dose hardness assurance.

SECTION III
DISCUSSION OF PHYSICAL MODELS AND HARDNESS ASSURANCE TECHNIQUES SUGGESTED BY THE MODELS

1. BASIC MECHANISMS OF TOTAL DOSE IRRADIATION

There are two long term phenomona resulting from the interaction of ionizing radiation with semiconductor device oxide which cause degradation of the electrical characteristics:

(1) Trapped positive charge in the oxide.

(2) Creation of additional interface states with energies near the middle of the silicon band gap.

Our current understanding of the physical mechanisms which give rise to these two phenomona is as follows. As ionizing radiation of sufficient energy (> 9eV) enters the oxide, electron-hole pairs are created. These free carriers will diffuse and/or drift toward the oxide boundaries depending on the direction and strength of an electric field in the oxide. Since the mobility of the electrons is much greater than that of holes, many of the electrons will be swept out before they can recombine with the hole they left behind (geminate recombination) or another hole (columnar recombination) (refs. 1, 2). The number of electrons which escape recombination (refs. 1-4) is a strong function of electric field. The holes left behind eventually get trapped in deep energy levels primarily near the SiO_2-Si interface or they escape into the silicon or aluminum (depending on the polarity of the electric field). The percentage of holes which escape recombination and become trapped in the oxide varies as a function of oxide processing parameters but is generally less than 10 percent for MOS gate oxides (refs. 1-3, 5).

The mobility of holes in thermal SiO_2 has been studied extensively, both experimentally and theoretically. Hole mobility is several orders of magnitude smaller than electron mobility. It is generally accepted that holes move through the oxide by hopping between shallow traps that are located fairly uniformly throughout the oxide. One suggestion is that the charge transfer mechanism is polaron hopping between randomly

distributed localized states (ref. 6). It has recently been discovered that holes can even become trapped in deep traps near the Si-SiO_2 interface under a negative gate bias when the holes are generated by VUV photons which are absorbed near the SiO_2-AL interface. To explain this phenomenon, the diffusion of neutral excitons has been proposed (ref. 7).

The increase in the mid-gap interface state density seems to occur after the holes are trapped near the interface. However, they appear nearly instantaneously for dry oxides and build up over a long time period (seconds to minutes) for wet oxides (ref. 8).

In addition to our understanding of the time, temperature, and electric field dependence of hole transport and trapping and interface state buildup, we know that it is not even necessary to irradiate a device to create these phenomona. By injecting holes into the oxide through nonradiation techniques (refs. 9-12), we observe hole transport and trapping with similar distributions as for ionizing radiation. Studies involving ultraviolet radiation (ref. 5) and low energy electrons (ref. 4) (where hole-electron pairs are created in only a portion of the oxide near the SiO_2-metal interface) along with hole injection studies (ref. 10) indicate that the deep level hole traps and the defects which give rise to additional interface states are not created by the radiation but are process-induced. The influence of processing on hole trap density, distribution, and capture cross-section has been studied and the critical steps indentified (refs. 13-15).

Although much has been learned about the phenomona of hole trapping and interface state generation, there are still some important unanswered questions:

(1) What is the nature of the hole trap? Are there many different types of hole traps involving both extrinsic defects (impurities) as well as bonding defects between silicon and oxygen?

(2) Does radiation create additional hole traps or are all hole traps process-induced?

(3) What process is responsible for the creation of interface states? Are they caused merely by holes crossing the interface? Does irradiation of the interface create additional states? Is the trapped charge near the interface necessary for the creation of interface states?

(4) What bonding defects are responsible for the "radiation" induced buildup of interface states? Are there several discrete energy levels or is there really a continuum of states as measurements might indicate?

In order to fit many of the experimental facts and to answer some of the preceding questions, several investigators have developed physical models of hole traps and interface bonding defects. In order to determine possible hardness assurance techniques, several of these models are discussed and possible measurements relating to the defects are identified.

2. MODELS OF HOLE TRAPS

a. Excess Silicon Hole Trap Model

During the thermal oxidation process at high temperature, oxygen diffuses through the oxide and interacts with the silicon to produce SiO_2 (ref. 16). When the oxide is cooled and oxidation ceases, an excess of silicon is left near the SiO_2-Si interface which extends 100-200 Å into (ref. 17) the oxide. Various bonding defects which arise from the nonstochiometric effects of the excess silicon have been proposed as the source of hole traps. Maier (ref. 18) proposed that silicon excess centers occur where one oxygen is bonded to three silicon atoms. Sah (ref. 19) refers to silicon excess centers as half oxygen vacancies or trivalent silicon. This defect is a donor having an energy in the SiO_2 bandgap slightly above the Si conduction band. Marquardt and Sigel (ref. 20) have performed ESR measurements to detect E' centers which result from oxygen vacancies in the oxide, similar to defects found in

bulk silica. The E' centers, however, are apparently produced by the irradiation indicating that the concentration of excess silicon may be enhanced by the radiation. Significant concentrations of gamma induced E' centers only occur at very high radiation levels (> 10^7rad(Si)). Thus, it is probably the process-induced excess silicon which are important for semiconductors irradiated in the 10^3-10^7 rad(Si) range.

If process induced excess silicon near the SiO_2-Si interface is responsible for hole trapping, the task of hardness assurance becomes one of measuring the concentration and hole trapping cross-section of these centers in a device or test structure. In order to be used as a screen, the test must be nondestructive and performed on critical oxides (i.e., gate oxides for MOS and base oxides for bipolar). As a sample test, it could be performed on a test wafer or special test structure located at various positions on a wafer.

Several attempts have been made to measure excess silicon centers in thermal SiO_2 grown on silicon. Mitchell and Denure (ref. 21) used cathodoluminescence to explore impurities and bonding defects in SiO_2. This method requires irradiation of the sample with a 5-10 KeV electron beam to produce luminescence spectra. The 450 nm peak in the spectra was attributed to trivalent silicon or oxygen vacancy. In order to obtain a good signal, the sample had to be irradiated to $\sim 10^9$ rads. Jones and Embree (ref. 22) present data supporting the contention that the 290 nm band is trivalent Si or an oxygen vacancy. They cite a recent paper by Koyama, Matsubara, and Mouri (ref. 23) which suggests that the 280 nm and 530 nm bands may be trivalent silicon. Thus it is not clear whether or not the cathodoluminescence technique can be used to identify the excess silicon center which has been proposed as the hole trap. A complete study would be required to correlate the amplitude of the various signals (as a measure of the concentration of the centers) with the amount of hole trapping resulting from radiation. This technique cannot be considered practical since it is a destructive technique which requires an irradiation of the sample. The irradiation itself causes additional

excess silicon centers which change the value of the parameter being measured. A sample radiation test on the actual device would be more practical and cost-effective.

Another method for measuring the concentration of excess silicon centers is the use of electron spin resonance (ESR). Poindexter (ref. 24) has provided evidence that the P_β center measured in the ESR spectrum is associated with trivalent silicon at the SiO_2-Si interface. However, this seems to be connected with the triply coordinated Si right at the interface which gives rise to interface states rather than the excess silicon in the bulk oxide near the interface which is associated with the hole trap.

It is not known whether ESR can detect the excess silicon which, according to this model, is associated with the hole trap. In any case, the use of ESR for measuring defect concentrations in thin oxides is not considered a viable production technique. The equipment is not geared to routine production sampling, and interpretation of ESR data is quite complex.

An indirect measure of any excess silicon related hole traps has been suggested by Maier (ref. 18). In his model, Maier suggests that Q_{ss} is a donor state with an energy level above the silicon conduction band. He further suggests that it consists of an oxygen atom bonded to three interface silicon atoms and its value immediately after oxidation, before annealing, is related to the rate of oxidation. Maier has developed a mathematical expresson for the density of hole traps (proposed to be due to excess silicon in SiO_2) as a function of oxidation temperature, oxide thickness, oxygen activity during growth, and the rate of oxidation. This expression suggests that the susceptibility of an oxide to radiation-induced hole trapping is proportional to Q_{ss} measured after oxidation, before annealing. Annealing the oxide in nitrogen or hydrogen can alter the value of Q_{ss} and distort the relation. Thus a measure of Q_{ss} during the processing on a test wafer may prove a useful test for trapped hole density.

b. Viscous Flow of SiO_2

A model to explain the origin of process induced hole traps has been presented by EerNisse and Derbenwick (ref. 25). They propose that microscopic shear flow occurs at the SiO_2-Si interface during high temperature processes from differences in thermal expansion of Si and SiO_2 and the viscous nature of SiO_2 at high temperature.

The stress relief which occurs during cool-down and subsequent processing introduces hole traps near the interface. While this model explains the effects of high temperature processing and the thickness dependence of the radiation induced damage, it does not address the nature of the bonding defects which result from the stress relief. However, the model does suggest a measurement which could be made to determine the radiation sensitivity of an oxide.

If one could measure the amount of stress before and after certain high temperature processes, stress relief could be determined. The only problem encountered is that stress relief during the actual oxidation process cannot be measured since there is no reference point. This means that only the additional stress relief from subsequent processing can be measured.

In terms of applying the technique as a hardness assurance tool, the method can only be used as a sample test and is impractical. EerNisse (ref. 26) has measured the stress relief resulting from anneals and found it to be a few percent of the total stress. This means that the measurement system must be very accurate for a quantitative analysis. Also, the oxide formed on the wafer backside must be removed after every high temperature process in order to measure only the stress resulting from the oxide of interest.

In conclusion, the shear flow model may explain the origin (if not the nature) of hole traps but does not suggest a practical hardness assurance technique which could be implemented either as a 100 percent screen or sample test.

c. Impurities (Extrinsic Defects)

One of the first models of oxide charge buildup is that the hole traps are due to impurities in the oxide, primarily sodium. Many different impurities are found in oxides (refs. 27-29) including sodium, hydrogen, potassium, copper, iron, carbon, and nitrogen. The mobility of sodium in SiO_2 is appreciable even at room temperature and ionzied sodium is known to cause electrical instabilities in heavily contaminated oxides. While the concentration of positively charged mobile impurities can be measured electrically using bias-temperature stresses, the radiation sensitivity has not been correlated to positively charged contaminants. The hardness has been correlated to total Na concentration in an experiment where Na was implanted in the oxide in controlled amounts (ref. 30). The concentrations however, were much greater than would normally be encountered in modern devices. It has not been experimentally determined that concentrations of impurities in the range found in modern devices correlate with the radiation sensitivity. However, if we assume that impurities (in certain bonding arrangements) can act as hole traps, the hardness assurance task is to measure their concentration before radiation on either devices or test wafers.

Since it is the total concentration and not the ionized fraction that is important, there is no known electrical measurement that would indicate the presence of impurities unless the impurity was responsible for an interface state. If the impurity were located very near the SiO_2-Si interface and gave rise to an interface state near the mid-gap of silicon, its presence could be detected using quasi-static C-V analysis. For neutral impurities not contributing to interface states, a physical analysis would be required to measure their concentration. Most analysis techniques (including ion microprobe, electron spin resonance, Auger, and x-ray photoelectron spectroscopy) are not sensitive enough to detect impurity concentrations typical of modern oxides. Also the equipment needed for the analysis is generally very expensive and not amiable to production testing. Another difficulty is that most impurities seem to be concentrated near the SiO_2-Si interface which makes their detection more difficult.

If a spectroscopic measurement were sensitive enough for concentrations of interest, they could not be used as a 100 percent screen, but would have to be implemented on a test wafer or special test structure. Also, quantitative standards have not been developed so that an accurate prediction could be made even if correlation were established between impurity concentration and hardness.

It is doubtful at this time if a practical solution exists for measuring small concentrations of impurities in thin oxides on a routine basis. Therefore, although the model may be valid for some processes, a practical means of implementing it for hardness assurance does not presently exist.

d. Interface Dipoles

A model for oxide charge proposed by Goetzberger, Heine, and Nicollian (ref. 31) and later expanded by Pepper (refs. 32-34) is that the total charge in the oxide is much greater than the net charge (usually positive). The bulk of the oxide charge consists of positive and negative charge pairs, or dipoles, which are located near the SiO_2-Si interface. C-V analysis of oxides only detects the presence of the net charge. Pepper (ref. 32) has conducted experiments to indirectly measure the number of dipoles and has shown that their number decreases in proportion to the increase in positive charge after irradiation. He concludes that the negative charges associated with the dipole are responsible for the hole trapping. The dipole density is measured by comparison of the preirradiation and postirradiation conductivity versus gate voltage of an MOS transistor at 4 K.

The presence of the dipoles causes random potential fluctuations near the SiO_2-Si interface which affects the low temperature channel conductance as a function of the distance between the carriers and the interface. Thus the conductance will change by a large amount if carriers are pushed closer to the interface. Pepper uses this observation to distinguish hard and soft devices. Hard devices will change very little

in conductance at 4 K with or without a substrate bias (to force carriers closer to the interface), whereas a large variation is observed on soft devices.

Thus a screen for hardness is immediately suggested by this model in the work of Pepper. The measurements however must be made at 4 K which precludes its use in a production environment. The problem for hardness assurance, if this model is valid, becomes one of devising a room temperature measurement which will correlate to the number of dipole charges in the SiO_2 near the interface. Pepper's measurements on both hard and soft devices indicate that at least half the holes trapped in the oxide cancel a negative charge associated with a dipole close enough to the interface to affect the channel conductance at 4 K.

A possible solution to the measurement of dipoles has been suggested by Maier*. The dipoles create a random fluctuation in surface potential which affects the distribution of allowable energy states of charge carriers. If the distribution of allowable states is broadened sufficiently, the tail of the distribution can extend into the silicon band-gap. This band tailing may be the source of interface states near the band edges. Thus, the density of states near the band edge may correlate to the number of dipoles, hence hole traps. The problem then becomes one of measuring edge states at room temperature. Possible solutions to this problem will be discussed in a later section.

Another approach to measuring the presence of dipoles near the interface is suggested in the work of Nicollian and Goetzberger (ref. 35) on the a-c conductance technique for measuring interface state density. They attributed the broadening of the a-c conductance of an MOS capacitor versus frequency to surface potential fluctuations from the <u>total</u> charge in the oxide. They developed a statistical model in which the standard deviation of broadening was related to total charge. In another paper Nicollian and Melchoir (ref. 36) applied this same theory to noise measure-

*NOTE: Private communication with Roe Maier.

ments on MOS capacitors. The standard deviation of the frequency range over which the noise voltage followed a 1/f dependence was related to total oxide charge.

Thus the dipole, or total charge model, suggests two approaches to a room temperature screen for hole trap density. In the indirect approach, the edge states are monitored as a measure of total charge. In the direct approach, either the frequency broadening of the a-c conductance or the frequency response of the noise is monitored as a measure of the total oxide charge. The total oxide charge less the net positive charge is then a measure of dipoles.

e. Silicon Surface Defects

A model which has been used to explain both increases in trapped charge and stretchout of the C-V curves is that of crystalline defects on the silicon surface (ref. 37). These defects are present after wafer slicing and surface preparation and are increased due to device processing. It has been established by H. Hughes (ref. 37) that within a diffusion lot, devices from wafers with different defect densities show different radiation response. The devices with higher defect density show a much greater stretchout voltage at flat band which, although it resembles the effect of interface states, is due in part to lateral nonuniformaties (LNU's) in the trapped positive charge (charge clusters). These charge clusters are thought to occur at the surface defect sites. Hughes proposes that oxidation induced stacking faults may be caused by silicon interstitials condensing at the fault site. These interstitials may be the hole traps at the interface which would give rise to LNU's. G. Hughes (ref. 28) has shown that even over the surface of a wafer, the defect density can vary greatly. His data indicate that a device with high defect density shows a correspondingly higher ΔV_{FB} than a device on the same wafer with a lower defect density. However, a quantitative relationship cannot be shown between the actual defect density count and the number of trapped holes (or stretchout due to clustering). Thus counting defect centers, which are revealed by various chemical etch techniques (Sirtle, Secco, and Wright), will apparently only indicate relative device hardness on a wafer or within a diffusion lot.

Since the uncompensated surface defects also correlate to surface carrier lifetime, two possible hardness assurance techniques are suggested by this model.

(1) Measure the surface defect density under the oxide of interest (gate oxide for MOS).

(2) Measure the surface carrier lifetime after oxidation but before any annealing.

Although the surface defect model may be useful in explaining one source of hole traps and charge clusters, it appears to be a first order effect only over a narrow range of devices. In studies at Sandia Labs, Derbenwick* has found that over a large number of diffusion lots and variations in process (for a controlled low value of preprocessing defect density), there was no correlation between the number of etch pit counts and ΔV_{FB} on test capacitors. This does not eliminate the possibility that within a lot the relative post-processing defect density may correlate to hardness, but it does indicate that the number of surface defects does not quantitatively predict hardness. Also Brown (ref. 31) has shown that for bipolar oxides where the extended high temperature operations introduce a large density of surface defects, there is no correlation between defect density and hardness.

In conclusion, since the surface defect density model is more readily verified than the other models, more data have been taken to determine its applicability. The results of these investigations indicate that at best, the model is only first order for a narrow range of devices (semi-hard MOS devices) and in this case can only be used as a relative indicator of hardness. Therefore its usefulness is quite limited.

3. MODELS OF RADIATION INDUCED INTERFACE STATES

a. Hydrogen

Several investigators including Sah (ref. 19), Revesz (ref. 38), and Svensson (ref. 39) have proposed that hydrogen at the SiO_2-Si interface

*NOTE: Private communication with Gary Derbenwick, presented at the ASTM Workshop on Defects in Materials, San Diego, Sept. 16, 1976.

is responsible for the buildup of mid-gap interface states from radiation. Sah (ref. 19) proposed that the ionizing radiation breaks a bond between trivalent silicon and a hydroxyl (OH), releasing the OH, which drifts toward a positive electrode. The fact that hydrogen is present in SiO_2 in large quantities has been shown even in "dry" oxides (refs. 38, 40). Although dry oxygen, used in dry thermal oxidation processing, is monitored for water content, it still is known to contain methane. At oxidation temperatures, the methane decomposes and hydrogen enters the oxide. Hydrogen is also present in dry processes from diffusion through the oxidation tube walls. Thus an appreciable amount of hydrogen may be present even in dry oxides, although it is certainly lower than in steam grown oxides. The fact that hydrogen is instrumental in producing interface states from irradiation may also be inferred from experiments with chlorine as a gettering agent. Chlorine is used to reduce sodium contamination in furnace tubes. It has also been used as a gettering agent during oxide growth. However, oxides grown in the presence of chlorine are known to be very susceptible to interface state buildup after radiation. Since chlorine will bond with silicon in much the same manner as OH, the effects of radiation may be similar for OH contaminated devices. Also a hydrogen anneal after oxidation is known to reduce the initial mid-gap interface state density. However, after irradiation, the increase interface state is much greater than for an unannealed device. Although the precise bonding arrangement for hydrogen may not be known (see combined model of Svennson), it appears that hydrogen is responsible for ΔN_{ss} from radiation. The hardness assurance problem then becomes one of measuring the hydrogen content of the oxide before radiation.

The only direct means of measuring H or OH content in thin oxides (identified in this program) is that of internal reflection infrared spectroscopy. Using this technique, Beckmann and Harrick (ref. 40) have measured profiles of H and OH in wet and dry oxides. However, as with other spectroscopic techniques, this method is not considered practical

for routine hardness assurance sampling. Such methods are also generally limited to wafer sampling which limits the technique to a sample test at the processing lot level.

It may be possible to infer the hydrogen concentration by measuring the preirradiation value of mid-gap interface states. If a lower limit can be established for a hardened oxide after oxidation, but before annealing, then a measured value of N_{ss} lower than this limit would indicate compensation of interface states by hydrogen or hydrogen-like species. Thus for a hardened process, increase in N_{ss} after irradiation may be inversely proportional to the initial N_{ss}. The practical limitation to using such a technique is that even with quasi-static measurements, the limit of detectability is usually $10^{10}/cm^2$. Greater sensitivity may be achieved using a gated-diode to measure the surface recombination velocity which is a direct function of the mid-gap N_{ss}. This technique will be discussed in a later section.

b. Trapped Charge Clusters

Another model of mid-gap interface state generation is that of Goetzberger, et al. (ref. 31), relating interface states to trapped charge. In their model, the interface states are attributed to the trapped positive charges. Single charges produce shallow states near the band edge. The deeper states near mid-gap are produced by clusters of several charges. If this model is accepted, a preirradiation screen would have to provide a measure of whatever phenomona gave rise to charge clustering.

A possible answer to this was presented in the surface defect model for charge trapping. It has been shown by H. Hughes that surface defects cause charge clustering which results in a stretchout of the CV curves. If the charge clustering also gives rise to mid-gap interface states, the stretchout is a compound effect which results from both charge clusters and the resulting interface states which the charge cluster creates. The fact that investigators have observed stretchout due only to ΔN_{ss} with no lateral nonuniformities suggests that this model is not valid or at least does not explain the majority of mid-gap states.

4. UNIFIED MODEL OF SVENSSON

The most recent model for the total dose response of thermal SiO_2 is a unified model by Svensson (ref. 39). In this model, the excess silicon model for hole trapping is combined with the hydrogen model for interface state generation. The model assumes three forms of trivalent silicon as shown in Figure 2. The surface trivalent silicon $Si_s^{\bullet}$ is bonded to three silicons. This is a dangling or unsaturated bond. In the oxide the two forms of trivalent silicon are $Si_o^{\bullet}$, a silicon bonded to three oxygens, and $Si_{os}^{\bullet}$ which is the same as $Si_o^{\bullet}$ except that it resides very close to the interface. $Si_s^{\bullet}$ is assumed to be a surface trap, $Si_o^{\bullet}$ a deep hole trap, and $Si_{os}^{\bullet}$ a very deep hole trap. The unifying aspect of the model is brought about by hydrogen. At the surface, hydrogen combines with $Si_s^{\bullet}$ to passify the surface trap. In the oxide, hydrogen combines with $Si_o^{\bullet}$ to form an Si_oH hole trap which, upon charging, gives Si_o^{+} + interstitial hydrogen (H_i).

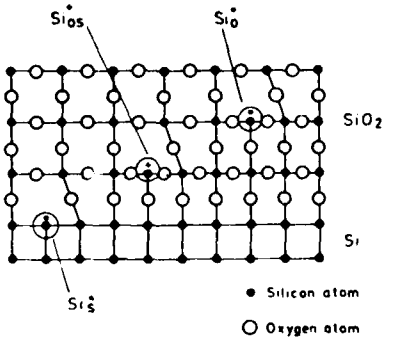

Figure 2. The Si-SiO_2 Interface With the Three Forms of Si$^{\bullet}$ Defects (Reference 39)

Using these concepts, Svensson has explained Q_{ss} in terms of Si_{os}^{+} and initial surface states in terms of $Si_s^{\bullet}$. In the radiation effects portion of the model, hole trapping is explained by either of the two processes:

$$\equiv Si_o + h_o^+ \rightarrow \equiv Si_o^+$$

or

$$\equiv Si_oH + h_o^+ \rightarrow \equiv Si_o^+ + H_i$$

Where h_o^+ is a radiation induced hole. The generation of new interface states occurs as a result of hole trapping in the oxide. The H_i resulting from the hole trapping at the Si_oH sites reacts with interface Si_sH centers to form H_2 which then migrates away from the interface.

If this combined model of hole trapping and interface state generation were accepted, the hardness assurance task would consist of monitoring the concentration of trivalent silicon and hydrogen at and near the interface. This problem has already been addressed in Subsections 3a and 3b.

5. SUMMARY

Various models of hole traps and interface state buildup have been discussed in an attempt to determine what hardness assurance screens might be suggested. By approaching the problem in this manner, many potential screens are suggested which have been explored by previous investigators. A list of the possible preirradiation hardness assurance techniques identified by consideration of the models is given in Table 1. These techniques along with all other techniques identified in the literature or by personal contact will be discussed in the following section in terms of their effectiveness and practicality.

TABLE 1. H/A TECHNIQUES SUGGESTED BY MODELS

Quantity to be measured	Techniques
Hole Traps	
Excess Silicon	● Cathodoluminescense ● ESR ● Q_{ss} Immediately After Oxidation
Oxide Stress Relief	● Change in Wafer Curvature
Oxide Impurity Content	● Spectroscopic
Dipole Density	● Substrate Bias Effect at 4 K ● Edge States ● Total Charge From a-c Conductance ● Total Charge From Noise
Surface Defect Density	● Etch Pit Count ● Surface Lifetime
Interface States	
Hydrogen Concentration	● Infrared Spectroscopy ● Initial Mid-Gap N_{ss}
Charge Clusters	● Etch Pit Count

SECTION IV
DISCUSSION OF HARDNESS ASSURANCE TECHNIQUES

Total dose hardness assurance techniques fall into five main categories:

(1) Preirradiation electrical parameters.

(2) Oxide and interface properties.

(3) Process and design controls.

(4) Stress tests which simulate radiation.

(5) Radiation tests.

The most desirable hardness assurance technique is to make a simple electrical test at the wafer level and from that measurement predict the postradiation response of the device. This is nearly the case with neutron damage in bipolar transitors, where the postirradiation current gain β_ϕ can be determined from the preirradiation current gain β_o through the relation,

$$1/\beta_\phi - 1/\beta_o = K\, t_b \phi$$

In order to predict β_ϕ one must measure β_o and the base transit time (t_b) as well as have a reasonable value of damage coefficient, K. The accuracy of the prediction depends on the extent to which the degradation is related to increases in the neutral base region recombination current after radiation, since the normalizing parameter, t_b, is a measure of the base width which is, in turn, proportional to the volume over which the recombination occurs. Thus, the method works best in the collector current region where the bulk base recombination current is dominant. Also, since K can vary with many fabrication variables such as doping density, dopant type and crystal growth method, the prediction formula works best if K is derived from a radiation test sample from the same device type and manufacturer.

Once these criteria are met, however, the relation provides a very good means of predicting postneutron radiation β from preirradiation electrical parameters.

Thus, an effort was made to identify studies which involved correlation between preirradiation electrical parameters and postirradiation response. However, considering the models of charge and interface state buildup, presented in the previous section, it appears doubtful that any simple electrical measurement would suffice.

Since the total dose radiation environment affects only the oxide and interface properties, a reasonable approach to hardness assurance would be to make direct measurements of surface properties, in order to find parameters which correlate to total dose response. Many investigators have devised special test structures to measure surface properties such as Q_{ss}, N_{ss}, oxide stress, and surface defect density. Probably the most universal of these structures is the MOS capacitor, from which a C-V analysis will yield Q_{ion}, Q_{ss}, and N_{ss}. Physical measurements such as oxide stress and silicon surface defect density generally require special test wafers to be run with each diffusion lot.

Total dose hardness is known to depend very strongly on processing and design parameters. Therefore controlling the design and process can be utilized as a hardness assurance technique. The major problem with this technique is that it can generally be implemented only by the manufacturer. There are very few, if any, tests that can be performed by a user which will tell him how the part was processed and to what degree it was controlled. Topographical analysis will indicate if design changes have been made.

Another approach to hardness assurance is to simulate the desired environment with an electrical and/or temperature stress test. This approach is used for EMP hardness assurance where the effect of the pulsed electromagnetic field is simulated by electrical pulses of appropriate voltage or current, duration, and shape. It may be possible to simulate the total dose environment by either electrical or thermal injection of holes into the oxide.

The final category of hardness assurance techniques is to actually irradiate the device and observe the degradation. In this approach, the

radiation source may be of any form that will cause a uniform deposition of ionizing radiation without creating an appreciable amount of displacement damage.

1. ELECTRICAL PARAMETERS

The easiest total dose screening technique would be to place limits on preirradiation electrical parameters and guarantee that the failure level of all parts meeting the electrical test limit would be greater than a specified amount. A search of the literature and discussions with several investigators uncovered only one electrical test with demonstrated correlation to total dose hardness. In tests performed both at NRL* and JPL (ref. 41) the increase in offset voltage on LM 108 op amps from one manufacturer was correlated to the operating current of the input transistors at the wafer lot level. Although unverified by tests, a potential electrical screen is 1/f noise on MOS transistors. This screening parameter was discussed in conjunction with the dipole model of hole trapping presented in Section III.

Because of the desirability of using preirradiation electrical parameters as screens several studies have been conducted to determine their correlation, or lack thereof, to total dose response. Most of the studies, for which published data exists, were conducted on bipolar devises. The results of these studies will be presented by parameter.

a. D. C. Current Gain and Base Current

Low current h_{FE} is one of the most sensitive bipolar transistor parameters to total dose. The maximum total dose induced increase in surface base current is due primarily to the increase in mid-gap interface state density (ref. 42) as shown by the expression:

$$I_{so} \approx \frac{1/2\ q\ n_i\ A\ N_{ss}\ \sigma\ V_{th}\left(e^{\beta V_{BE}} - 1\right)}{e^{\beta V_{BE/2}}\ \cosh\ \beta\left[\phi_s - \phi_o - \phi_F + \frac{V_{BE}}{2}\right]}$$

NOTE: Private communication with Les Palkuti.

The major effect of the positive charge buildup in the oxide is to increase the surface potential, ϕ_s. If the positive charge in the oxide becomes sufficient to invert the p region (base of an npn transistor) a field induced junction can occur which extends the E-B junction across the base surface. This adds a space charge recombination current to the base current. However, in most bipolar transistors at doses of 10^6 rads or less, this does not occur because the base surface doping is sufficiently high to prevent inversion. Therefore, the primary effect is the increase in I_{so} from increases in N_{ss}.

Although several investigators have sought a correlation between the initial value of h_{FE} and the increase in h_{FE} from total dose, published results could only be found in one study (ref. 43) (See Table 2). In that study rank correlation coefficients (indicative of relative sensitivity) were determined for h_{FEO}, base surface current, I_{BS}, and change in base surface current from burn-in correlated against various indicators of radiation sensitivity, e.g.,

$$h_{FE}(\gamma),\ \Delta h_{FE},\ \frac{h_{FE}(\gamma)}{h_{FEO}},\ \text{and}\ \Delta 1/h_{FE}.$$

The results are shown in Table 2. Although a consistently high rank correlation between h_{FEO} and Δh_{FE} was observed, Δh_{FE} is not the true indicator of hardness, as was pointed out. Correlation between h_{FEO} and $\Delta 1/h_{FE}$ was not good, the highest rank correlation coefficient, r, being .6 to .7 for a 2N2905A. For the other two transistor types studied, r was .2 to .6.

In a study by this author on 2N2222A's, unranked correlation of 0.5 to 0.8 was observed for h_{FEO} versus $\Delta 1/h_{FE}$. Also a screening level could be set on h_{FEO} to eliminate all devices with the largest $\Delta 1/h_{FE}$'s. However, this study was limited to about 25 devices from one manufacturer. The fact that isolated cases of reasonable correlation are found for a parameter does not justify its use. For a parameter to be acceptable as

TABLE 2. RANK CORRELATION COEFFICIENTS FOR TOTAL DOSE DAMAGE PREDICTION (REFERENCE 43)

X vs. Y (a)	2N709	2N930	2N2905A
(1/f) Noise	0.3	0.2	0.3
I_B° vs. I_B (dose)	0.5-0.94	0.35-0.7	0.96-0.97
I_B° vs. I_B/I_B°	-(0.6-0.4)	-(0.3-0.2)	0.8-0.7
I_B° vs. I_B(dose)-I_B°	0.2-0.65	0.2-0.4	0.6-0.7
$1/I_B^\circ$ vs. I_B° - $1/I_B$)	0.91-0.94	0.97-0.8	0.98-0.96
ΔI_B (low injection) vs. ΔI_B (high injection)	0.96-0.55-02	0.98-0.90	0.90-0.80-0.55
h_{FEO} vs. h_{FE}(dose)	0.56-0.80-0.96	0.36-0.49-0.68	0.97-0.97
h_{FEO} vs. h_{FEO}-h_{FE}(dose)	0.91-0.94	0.97-0.83	0.96-0.95
h_{FEO} vs. h_{FE}/h_{FEO}	-(0.6-0.4)	-(0.3-0.2)	-(0.8-0.7)
h_{FEO} vs. $\Delta h_{FE}/h_{FEO}$	0.5-0.6	0.3-0.2	0.8-0.7
$1/h_{FEO}$ vs. $\Delta(1/h_{FE})$	0.2-0.7	-(0.4-0.2)	-(0.7-0.6)
I_B°	-0.5	-(0.6-0.55)	0.7-0.85
I_B° (T)	-0.4	-0.4	0.7-0.8
ΔI_B (due to ΔT)	0	-0.3 to 0.3	-(0.3-0.2)
I_{EBO}° (or BV_{EBO}°)	-0.4	-0.3	0.6-0.75
I_{EBO}° (T) (or BV_{EBO}°)	-0.4	-0.3	0.6-0.75
ΔI_{EBO}(due to ΔT)(or ΔBV_{EBO})	-0.4	0.2	0.6-0.7
ΔI_{EBO} (due to burn-in)	0	---	---
2N930 (1/f) Noise	---	0.3	---
Pre- I_B°	---	-0.4	---
burn-in I° (T)	---	-0.4	---

a hardness assurance screen, it must work from device to device, vendor to vendor, and lot to lot. In addition, it should have a sound physical basis to lend theoretical support. In the case of h_{FE}, there are no analytical grounds, based on recent models of hole trapping and interface state generation, to support a relationship between initial base surface current and increased base surface current except for the possible inverse relation between N_{ss} and ΔN_{ss} discussed in Section III.

For bipolar oxides, the potential relationship between N_{ss} and ΔN_{ss} due to hydrogen passivation of the surface states may be a second-order effect. According to this model, devices with the smallest initial value of bulk base surface recombination current should experience the largest ΔI_B hence $\Delta 1/\beta$. It is not clear that such a correlation has ever been investigated. In a study by Brunncke, et al. (ref. 44), an attempt was made to look at the correlation between $\Delta 1/\beta$ and initial base surface current. However, the test structure used for separating the surface current component (bipolar tetrode) did not give useful results. In the Boeing study (ref. 43), it was claimed that the h_{FE} tests were made at sufficiently low currents that surface effects dominated, but the surface term was not specifically determined.

The major problem with measuring the surface component of base current is in the quantity of data required and the data analysis. A complete plot of I_B versus V_{BE} is required at currents as low as picoamps. Even if such a plot is obtained, it is not always easy to pick out the portion of the curve having the proper slope for the surface component. For this reason, special structures such as the bipolar tetrode have been developed. However, if the use of special test structures is required to measure the base current, then one no longer has a simple preirradiation electrical parameter screen for the transistor. A means of measuring the surface recombination velocity using a gated diode will be discussed in a later section.

As the Hart, et al. (ref. 42) study has shown, based on the work of Reddi, a prediction of the increase in base surface current in

bipolar transistors must involve a prediction of both N_{ss} and the variations in base surface potential from the trapped positive charge distribution. Therefore, a measure of initial base surface current will at best only indicate changes in N_{ss}. The total change in I_B resulting from radiation may be due primarily to changes in ϕ_s, in which case no correlation would be expected for I_{BS} and $\Delta 1/\beta$.

b. Other Transistor Electrical Parameters

In the Boeing study, several parameters other than those relating to h_{FEO} were investigated, primarily measurements involving emitter-base leakage current, I_{EBO}, and 1/f noise. Neither of these parameters demonstrated reasonable rank correlation to radiation sensitivity, which is not too surprising since a good rationale cannot be presented for either parameter, as they were measured in the study. The possibility of using noise on an MOS device as a prediction of radiation induced trapped holes, Q_r, has been mentioned. Such a technique would involve either measuring the low frequency noise at the band edges or integrating the noise spectrum over the range where a 1/f dependence is observed. The use of these measurements of noise are based on the dipole theory of hole trapping. Such noise measurements cannot be made on ungated bipolar transistors. Also, even if a prediction of Q_r using noise measurements on bipolar devices were available, the major contribution to degradation in bipolar transistors is ΔN_{ss}. Thus, I_{EBO} and noise are rejected as effective bipolar transistor screens on the basis of both analysis and data.

Although it has not been published, one other transistor electrical parameter has been investigated rather extensively as a potential screen for maverick devices. Maverick behavior has been observed quite often in total dose testing and has been shown to be reproducible (ref. 45) after annealing and reirradiating. One possible explanation for the maverick behavior is the existence of large surface defect centers in the base, near the emitter base junction. After irradiation, these centers are the sites of large concentrations of trapped charge and recombination centers which give rise to anomalously high base surface currents. In order to

detect the existence of these defect centers before irradiation, Maier* has made measurements of the reverse bias characteristics of the emitter-base junction. As the E-B reverse bias is increased, the depletion region spreads into the base. When it passes across a large defect center on the base surface, one should observe a sharp increase in I_{EBO}. Maier characterized a number of 2N2222A devices, but did not observe any "maverick" behavior in total dose response. He then characterized 200 JFET's of a type which had shown maverick behavior in previous studies by JPL. The mavericks showed μA leakage currents after 10^6 rad(Si) whereas the normal postirradiation value was in the low nA range. Of the 200 devices tested by Maier, only one device showed a leakage current in the μA range and there was nothing peculiar in its preirradiation junction breakdown characteristic.

Based on these results, abnormalities in the reverse I-V characteristics of bipolar or JFET junctions cannot be considered an effective screen.

c. MOS Electrical Parameters

No publications were identified which discussed the results of any correlation studies between preirradiation MOS electrical parameters and radiation sensitivity. However, several investigators indicated that they had looked for correlations, mainly with initial threshold voltage, and had gotten no positive results. This is not surprising, considering our present understanding of the basic mechanisms. The only parameter which might show a correlation, as suggested by the dipole model of hole trapping, would be a measure of total oxide charge such as might be derived from noise or ac conductance measurements. These parameters will be discussed in detail under the section on total oxide charge.

Thus, with the possible exception of 1/f noise, it is concluded that there are no preirradiation MOS device electrical parameters which can be used as effective hardness assurance screen for total dose.

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*NOTE: Private communication with Roe Maier.

d. Input Transistor Operating Current on Linear IC's

Experimental data have shown that the degradation of current gain, h_{FE}, in bipolar transistors is very sensitive to the operating current. This dependence results from the fact that the increase in the surface component of base current does not exhibit an $e^{\beta V_{BE}}$ dependence as does the collector current, but rather a dependence given by

$$e\left(\frac{\beta V_{BE}}{n}\right)$$

where n = 1.5 - 2.

This results in a total dose degradation ($\Delta 1/h_{FE}$) which is greater at lower currents.

Because of this, the input transistors on bipolar linear IC's should experience a greater gain degradation if they are operated at lower collector currents. This is the basis for a screen which has been implemented by JPL (ref. 41) and NRL on LM 108 operatonal amplifiers. Since the offset voltage of an op amp is sensitive to changes in gain of the input transistors, devices having a larger $\Delta 1/h_{FE}$ from total dose will experience a larger ΔV_{off}.

The idea of using the input transistor operating current as a screen came from the work of Johnston and Skavland (ref. 46) who have used I_1 as a neutron effects screen. The neutron damage coefficient, K, is also quite sensitive to operating current. The use of I_1 as a screen for total dose effects on IC's assumes that within a given diffusion lot of devices, the variations in $\Delta 1/h_{FE}$ of the input transistors from IC to IC at a given operating current will be small compared to the variations in $\Delta 1/h_{FE}$ over the range of operating currents observed. If this is true, then one should see a reasonable correlation between I_1 and ΔV_{off}.

Figure 3 is an illustration of the variations which might be observed in the input transistor $\Delta 1/h_{FE}$ versus operating current. In this example, the expected variation in $\Delta 1/h_{FE}$ at the average operating current, Δ_1, is smaller than the variation in average $\Delta 1/h_{FE}$ over the range of operating currents. If this is the case, then the technique

should work as a screen for total dose degradation of input offset voltage, assuming that $\Delta 1/h_{FE}$ correlates to V_{off}. However, if Δ_1 is comparable to or larger than Δ_2, the screen will be ineffective.

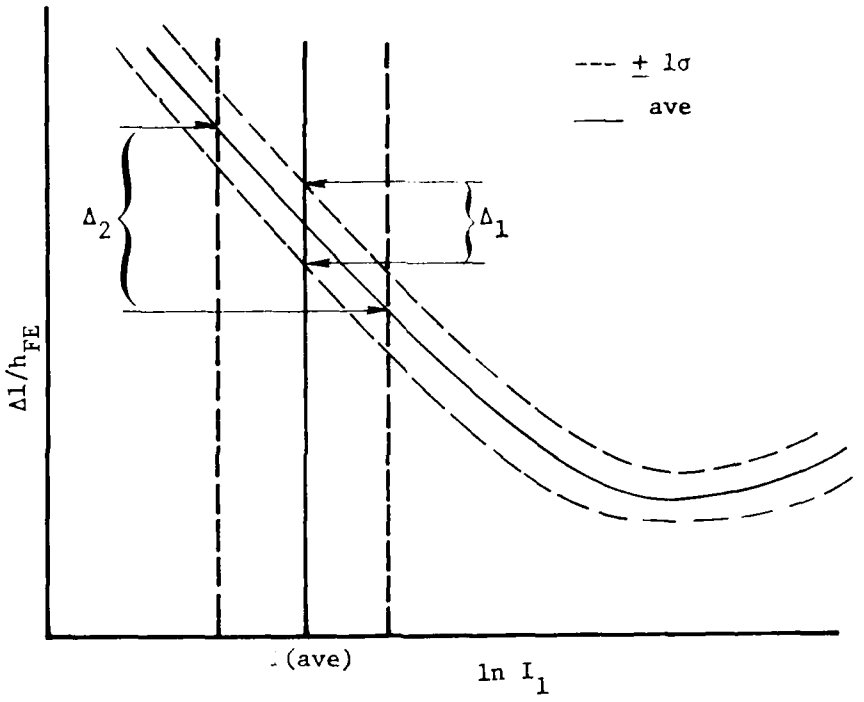

Figure 3. A Hypothetical Plot of $\Delta 1/h_{FE}$ Versus I_1 for op amp Input Transistors

Although the data taken by JPL (ref. 41) on about 20 LM 108A's representing several diffusion lots did not yield a high value of correlation coefficient (r was .63) they were able to determine good and bad lots consistent with the results by NRL based on different samples from the same lots. Although these data are limited, the technique appears to be promising, especially in those cases where I_1 can easily be measured through existing external pins without a redesign of the metallization. In order to determine how well the technique works on circuits other than

the LM 108, verification tests will be performed on two or three linear circuits with access to the input transistor emitter current. If the method proves effective with the additional device types, it will be pursued in the evaluation phase.

2. OXIDE AND INTERFACE PROPERTIES

The second approach to hardness assurance for total dose effects is to measure, either directly or indirectly, properties of the $Si-SiO_2$ interface or the SiO_2 film whose preirradiation value correlates to the radiation sensitivity. Many properties of the SiO_2 and $Si-SiO_2$ interface have been measured and their correlation to hardness investigated. Direct measurements generally involve a spectroscopic analysis to measure either intrinsic or extrinsic defect densities, whereas indirect methods generally involve electrical measurements on special test structures to infer interface or SiO_2 properties. This category differs from the electrical parameters in that a measure of specific interface or oxide properties cannot usually be extracted from specification terminal electrical parameters on devices or circuits.

a. Oxide Impurities

Extrinsic defects or impurities in the oxide are one possible source of radiation sensitivity. The discussion of impurities will be divided between contaminants which potentially add to the oxide positive charge after irradiation, either as mobile positive ions or hole traps, and impurities which result in increased interface state density after irradiation. The first category involves sodium, potassium, and other possible contaminants, whereas the second category involves hydrogen, hydroxals, and possibly chlorine.

(1) Impurities Contributing to Net Positive Charge

One of the most predominant and electrically active impurities in SiO_2 is sodium. Mobile ionized sodium caused instabilities in early MOS devices which resulted in a severe limitation of their usefulness. Contamination control measures such as cleaning oxidation tubes with HCl,

reducing contamination levels in all chemicals used in the process and increasing the cleanliness requirements for processing personnel has resulted in positive mobile ion concentrations of less than $10^{12} cm^{-2}$ for most commercial MOS products.

The role of impurities in hole trapping in the oxide is not clear. It is known that even "hard" oxides contain a variety of impurities. Grunthaner and Maserjian (ref. 27) have shown the presence of copper, iron, sodium, potassium, carbon, and nitrogen. G. W. Hughes (ref. 28) has shown the presence of chromium, chlorine, sulfur, aluminum, and trace amounts of still other elements in addition to those seen by Grunthaner and Maserjian. The most electrically active impurity however is probably sodium, and consequently most research has been conducted on the correlation of hardness with preirradiation sodium concentration. No correlation has been shown between preirradiation mobile sodium (in concentrations < 10^{12} cm^{-2}) and hardness (refs. 47, 48).

However, in ion-implantation studies, H. L. Hughes (ref. 30) has shown a correlation between the flat-band voltage shift on MOS capacitors and the total sodium concentration as shown in Figure 4.

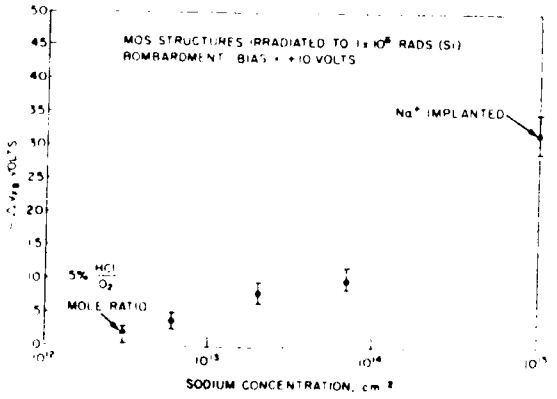

Figure 4. Radiation-Induced Flat-Band Voltage Shifts for MOS Structures of Various Sodium Levels (Reference 30)

Also Repace (ref. 49) has shown that Co^{60} irradiation can result in an increase in the mobile sodium concentration in a field oxide where the total Na concentration is higher. The total sodium concentration can be significantly larger than the mobile sodium concentration. Thus if the sodium is electrically neutral, being tied up by a nonbridging oxygen, it can be released by ionizing radiation and become positively charged. Data by Bhar, et al. (ref. 50), have shown that for gate quality oxides, 20 KeV electron irradiation from an SEM does not result in the creation of any significant number of additional mobile sodium. This is consistant with the data of Repace who only observed the increase in mobile sodium in field oxides. In the report by H. L. Hughes (ref. 30) it is not clear whether or not the ΔV_{FB} was due to mobile sodium or trapped holes. The only other data in which a possible correlation was drawn between hardness and impurity content are that of G. W. Hughes (ref. 28). Wafers representing hard and soft oxides were run through a spark source mass spectroscopic analysis and the impurity content of various elements measured. In this method, about 5 μm of material is vaporized from the wafer surface. Therefore the SiO_2 is only a small fraction of the total material analyzed, limiting the sensitivity. However, for one set of hard and soft wafers, presumably with thicker oxides, the sensitivity was great enough to measure a significant difference in impurity content. For this set of wafers the soft oxide (ΔV_{FB} = 4.9V @ 10^6 rad(Si)) had significantly higher concentrations of Cr, fe, Mn, K, and Cl than the hard oxide (ΔV_{FB} = 1.55V @ 10^6 rad(Si)). These data are shown in Table 3. Although these two wafers came from independent runs, it is assumed that they were processed in a similar manner such that the major difference is the contamination of the one sample. The contamination was attributed to a suspected HCl leak in a stainless steel gas line.

From the scant data presently available, it appears that significant impurity concentrations of certain elements (notably sodium and potassium) will degrade total dose hardness, although the exact mechanisms are still not clear. However, impurities are only one of many factors that contribute to soft oxides. In a hardness assurance program,

TABLE 3. IMPURITY ANALYSIS BY SPARK-SOURCE MASS SPECTROMETRY OF HARD AND SOFT OXIDE (Reference 28)

Sample 09136F ΔV_{FB} = 1.8 V			Sample 09136E ΔV_{FB} = 4.8 V			Sample 08046A1 ΔV_{FB} = 1.55 V			Sample 03056F1 ΔV_{FB} = 4.9 V		
Element	Conc. (ppma)	Error (%)	Element	Conc. (ppma)	Error (%)	Element	Conc. (ppma)	Error (%)	Element	Conc. (ppma)	Error (%)
Si	10^6	± 6	Si	10^6	± 3	Si	10^6	± 24	Si	10^6	± 16
O	1750		O	3930	± 37	O	17,100		O	14,600	± 105
Cr	0.174		Cr	0.08		Cr	0.253		Cr	1.20	± 73
Cl	1.63		Cl	1.43		Cl	1.23		Fe	7.45	
F	2.60		F	0.167		S	10.0		Mn	0.357	
C	12.8	± 90	C	20.8	± 42	Al	0.780		Ca	0.59	
B	0.027		B	0.105		F	0.598	± 8	K	6.29	
						C	148.0	± 67	Cl	5.52	± 78
Mn	<0.03		Mn	<0.07		B	0.238		S	10.9	± 58
Fe	<0.77		Fe	<1.65					P	0.498	
Ca	<0.12		Ca	<0.26		Mn	<0.063		Al	2.86	
K	<0.25		K	<0.53		Fe	Δ1.62		F	2.03	± 71
S	<4.0		S	<1.15		Ca	<0.242		C	69.5	± 243
P	<0.10		P	<0.198		K	<0.496		B	0.267	
Al	<0.09		Al	<0.18		P	<0.202				
Mg	<0.82		Mg	<1.72		Mg	<1.69		Mg	<1.04	
Na	<0.16		Na	<0.351		Na	<0.33		Na	<0.206	

impurity content of oxides should be monitored and kept below certain acceptable levels, as a safeguard against unsuspected contamination sources. The problem is one of a cost-effective, practical means of measuring impurity content. Electrical methods, such as high temperature bias and quasistatic C-V analysis on MOS capacitors, is limited to measuring mobile ion density and impurities at the interface which give rise to interface states in the silicon mid-gap region. Neither of these electrically active defect concentrations have been shown to correlate to radiation hardness. Therefore, a spectroscopic technique would be required that would have adequate sensitivity to measure concentration on the order of 10^{11} to $10^{13} cm^{-2}$ in 1000 Å oxides. Since gross contamination is generally lot-dependent, the analysis could be implemented by sampling one or two wafers per run. This would greatly simplify the spectroscopic analysis, since individual die or even wafer level qualification would be extremely difficult, if possible, and probably cost-prohibitive. Possible spectroscopic methods are ESCA, Auger, ion microprobe, and ESR. All of these techniques require expensive equipment and are not well suited to production sampling. In addition, at the contamination levels important for total dose effects, these techniques are not sufficiently quantitative.

(2) Impurities Affecting Interface State Generation

In profiling studies on various impurity distributions in SiO_2, using ion-microprobe (ref. 30), chemical etching (ref. 27), and multiple internal reflection infrared spectroscopy, (ref. 40) a U-shaped distribution of impurities is generally observed with a significant pile up at the Si-SiO_2 interface. Therefore, it is reasonable to assume that many impurities may contribute extrinsic defects that give rise to interface states. Many of these defect centers have energy levels near the silicon mid-gap. The impurity considered by many researchers (refs. 19, 38, 39) to be a major cause of the post-irradiation interface state density near mid-gap is hydrogen, primarily in the form of SiH. Sah (ref. 19) proposes that interface states are caused by ionizing radiation according to the relation

$$\equiv Si - OH + Rad \rightarrow \equiv Si \cdot + OH$$

He proposes OH as the likely species rather than H, because of the field dependence of the interface state buildup. The negatively charged OH^- will drift away from the interface under positive bias, whereas a positively charged H^+ will not. Profiles of H and OH concentrations, however, indicate an increase in H near the $Si\text{-}SiO_2$ interface (steam and dry oxides) and a decrease in OH (steam oxide) near the interface. The model by Svensson (ref. 39) resolves this inconsistency. In Svensson's model, the interface states are caused by trivalent silicon that is bonded to three interface silicons, $\equiv Si_s^{\cdot}$. This active surface trap is passified by a hydrogen to become $\equiv Si_sH$. Hole traps near the interface result from trivalent silicon in the oxide which is bonded to three oxygens, $Si_o^{\cdot}$. This hole trap can also be of the form Si_oH in which a hydrogen is held at the $\equiv Si_o^{\cdot}$ site. When holes, generated by ionizing radiation or injected into the oxide, are trapped at the $\equiv Si_oH$ sites, interstitial hydrogen, H_i, is released. This H_i reacts with $\equiv Si_sH$ to create an interface state, $Si_s^{\cdot}$, and H_2 which drifts away. This model explains why interface states are created when holes are trapped near the interface.

Whether or not this model is valid, or perhaps another model involving hydrogen, is not as important to a hardness assurance program as the fact that hydrogen is present in all SiO_2 films and plays a definite role in interface state generation. The hardness assurance problem is one of determining a practical means of measuring H concentration and establishing the quantitative correlation between H and postradiation interface state density. Data on the correlation have loosely been established by Revesz (ref. 38) and Derbenwick (ref. 47), et al. However G. W. Hughes (ref. 28), presents data showing no effect of H_2O concentration on the ΔV_{FB} of "dry" oxides from 16-50,000 ppm. In the work by G. W. Hughes, no H profiling was done on the low H_2O concentration oxides to determine the H concentration at the interface. Further work is required to establish a quantitative relation between H concentration at the $Si\text{-}SiO_2$ interface before irradiation and ΔN_{ss} (mid-gap).

As with the impurities discussed previously in subsection (1), the only means of measuring the H concentration is with elaborate and expensive spectroscopic techniques. No simple electrical measurement is known that will indicate SiH concentration, since it is neutral. A method does exist for accurately measuring the mid-gap interface state density using a gated diode. This method* is sensitive to very low values of N_{ss} (10^8 - 10^{9} cm^{-2}) for properly designed test diodes. To overcome the instrumentation problem of reading picoamp currents on the gated diode, the National Bureau of Standards (NBS) is working on a gated diode with an on-chip FET amplifier. The amplification factor is such that the readout is in volts for picoamp currents. This structure is being adapted for rapid wafer probe analysis.

Although the prerad value of N_{ss} (mid-gap) is not a direct measure of SiH concentration, there should be an inverse relation between N_{ss} and SiH concentration. Because of the inherent bonding defect structure between the crystalline Si and amorphous SiO_2, a large concentration of N_{ss} will exist even after high temperature anneals unless passified by an impurity such as hydrogen. Therefore, the lower the value of N_{ss}, the higher the impurity concentration at the interface. If this impurity is hydrogen and the proposed mechanisms are in effect for the release of hydrogen and consequent activation of the defects, then one should measure the inverse relation between N_{ss} and ΔN_{ss}.

The more direct approach, that of spectroscopically measuring the interface SiH concentration, is not well suited for production line procedures. Because of the difficulty of determining the concentration of H in SiO_2 spectroscopically, the indirect method of measuring N_{ss} (mid-gap) will be evaluated in this program.

b. Surface Defect Density

As discussed in the section on models, defects on the silicon wafer prior to oxidation or process-induced surface defects may be reasonable for hole trapping and clustering of trapped holes. The published data on

*NOTE: Private communication with Gary Carver.

the correlation of surface defect density and hardness are not extensive. H. L. Hughes (ref. 51) presented data on CMOS processes from five different vendors in which he compared the Sirtl etch pit counts per cm^2 to the radiation level required to induce a -1V ΔV_{TH} in n channel transistors in CMOS circuits. The data are reproduced in Table 4. The surface defect densities were determined on monitor wafers which accompanied each lot. The two data points on Vendor I are representative of devices processed at two different facilities having different specifications on starting material. The etch pit densities given in Table 4 are determined after processing and so include the residual damage after surface preparation and the process-induced damage. Derbenwick, et al. (ref. 47) investigated the

TABLE 4. SURFACE DEFECT DENSITY VERSUS RADIATION FAILURE LEVEL (REFERENCE 51)

Vendor	Sirtl etch counts cm^{-2}	Radiation Dose, Rads(Si) (for ΔV_{TN} = -1V, V_G = +10V)
Vendor I, Facility A	$2x10^3$	$2x10^5$
Vendor I, Facility B	$1x10^4$	$3x10^4$
Vendor II	$>10^5$	$3x10^3$
Vendor III	$5x10^4$	$1x10^4$
Vendor IV	$<10^2$	$>1x10^6$

relation between the surface defect density on the starting material and the radiation hardness. They concluded that the surface defect density had a significant effect on the initial interface state density and the radiation sensitivity. The surface defect density and, hence, N_{ss} and

the radiation induced ΔN_{ss} could be greatly improved by growing an 8000 Å oxide and stripping it or etching the surface in HCl vapor. The most improvement was seen using the HCl vapor etch. More recent unpublished studies by Sandia Labs, in which the post-processing etch pit density was determined as a function of ΔV_{FB} and MOS capacitors, indicate that no correlation exists between the actual etch pit count and ΔV_{FB} over several hundred wafers lots in which many processing variables were introduced. However, in this study, controls were placed on the starting material such that only very low defect density wafer starts were used. Such data would indicate that while a high defect density in the starting material will definitely degrade the hardness, the process induced defect density on low defect density starting material does not correlate with hardness.

Further studies by H. L. Hughes and King (ref. 37) indicate that the surface defects give rise to radiation induced lateral nonuniformities (LNU's) in the trapped positive charge, as well as increases in interface state density. They present data on two wafers which were fabricated in a common lot. However, the wafers come from different sources of starting material. There were apparently no differences in the defect densities of the wafers before oxidation. The post-processing etch pit density was measured and compared to the stretchout voltage, V_{ST}, after 3 X 10^5 rad(Si) (V_G = +10V during irradiation). Results are given in Table 5.

TABLE 5. DEFECT DENSITY VERSUS V_{ST} (REFERENCE 37)

Defect Density	V_{ST}(3 X 10^5 rad(Si), V_G = +10V
Wafer 1 113 ± 30	-2.27 ± .12
Wafer 2 2270 ± 725	-16.55 ± 1.2

The conclusion seems to be that different sources of starting material with the same initial defect density can result in different post-processing defect densities even though the processing is identical. In addition, it is the pre-processing defect density that correlates to hardness.

In this same paper, data are presented relating the radiation induced stretchout voltage to the silicon surface lifetime measured after oxidation but before any annealing. These data are reproduced in Figure 5.

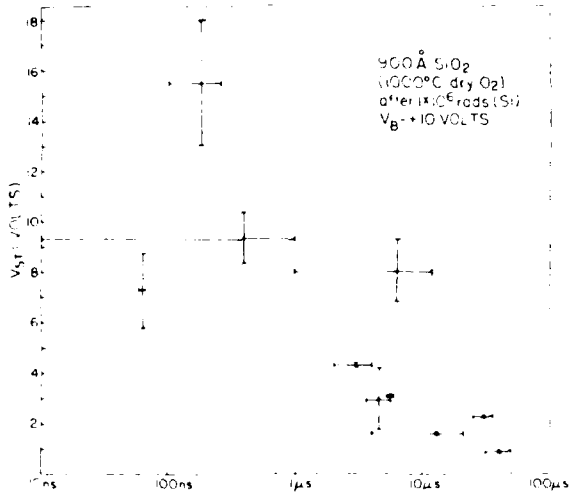

Figure 5. Radiation-Induced Stretchout Versus Surface Lifetime (Reference 37)

G. W. Hughes (ref. 28) has also determined the variations in defect density and hardness for two wafers within the same run. Using Secco etch techniques and counting only saucer-pits which are due to oxidation-induced stacking faults, he found that for the run with the largest wafer to wafer variation in ΔV_{FB}, there was good correlation between ΔV_{FB} and etch pit density. The data are given in Table 6.

TABLE 6. WAFER TO WAFER VARIATIONS IN DEFECT DENSITY AND HARDNESS (REFERENCE 28)

Device	ΔV_{FB} (V)	V_{st} (V)	Saucer pit density (cm^{-2})
09136E	4.8	0.7	1.74×10^5
09136F	1.8	0.2	6.21×10^4

However, he argues that the number of etch pits after processing is not a screen for hardness. Comparing the hardness of the oxides he measured to those of H. L. Hughes (ref. 37), there is an order of magnitude difference in the predicted radiation level to cause a 1V ΔV_{FB} based on the pit count. Therefore, within a given process, the etch pit density may be a good relative indicator of hardness but it does not appear to be a good screen.

Brown (ref. 48) has conducted an extensive study of the relation between process-induced etch pit density and hardness on bipolar processing. In a systematic study of the processing variables which affect linear bipolar total dose hardness, he subjected wafers from each process variation to sirtl etch and compared the pit density to ΔN_{ss} (as determined from MOS test capacitors). He consistently found no correlation between etch pit density, which ranged from a few hundred counts/cm^2 to 10^6 counts/cm^2, and either ΔV_{FB} or ΔN_{ss}. He observed a large variability in the pit count across a single wafer. The gross variability appeared as concentric rings of high density defects sometimes referred to as swirl. Therefore, he recorded the etch pit density in regions of both high and low density. No correlation to hardness was observed for either value. Although he observed a large variation in etch pit density on a single wafer, the hardness of the capacitors on the same wafer varied by a small amount (only one-half of the wafer was etched in most cases).

These results could be explained if it is the defect density of the starting material rather that the process induced defect density that is more relevant to hardness. In his studies, Brown used wafers from a single dedicated crystal for all the processing. Therefore, a minimum variability can be assumed for the defect density of the starting material. In addition to the control on the wafer source, all wafer surfaces were prepared in the same manner, except for one experiment designed to measure the effects of surface preparation on hardness. Using oxidation and stripping, chemical polishing, and mechanical-chemical polishing, no difference was observed in hardness compared to the normal epitaxial surface used in bipolar processing. There was however a marked difference

in swirl with the epitaxial and chemical polished surfaces showing no swirl and the oxidation-strip surface have marked swirl.

Another factor which could affect the comparison of these results with MOS processing results is that all wafers were <111> rather than <100>.

It is very difficult to draw any reasonable conclusions from the aforementioned data base that can be applied to a hardness assurance program. It does seem reasonable that (especially for MOS processing) controls should be placed on the surface defect density of the as-received wafers in order to increase the probability of producing "hard" devices. It is not clear that the flat-band voltage shift for a particular oxide can be related to the surface defect density, although within a given processing lot, the defect density may be a relative indicator of hardness.

As a hardness assurance technique, controls should be placed on the starting material in the form of an acceptance limit on the number of defects/cm^2. Based on the Sandia results, this limit can be applied after surface preparation. Because of the amount of processing required to develop a reasonable acceptance limit, this technique will not be evaluated in this program. The limits should be determined by each vendor for his own process.

c. Initial Oxide Charge

After processing a thermal oxide on silicon, there remains a fixed positive charge, Q_{ss}, in the oxide near the interface that cannot be annealed out with a low temperature (300-500°C) anneal. Even though it has been reported to be located within 20Å of the oxide, as determined by photoinjection techniques (ref. 52), it cannot be removed by tunneling of charge carriers from the silicon. Q_{ss} can be significantly reduced by a nitrogen anneal at high temperatures (900-1200 °C). However, as shown by Deal (ref. 53), an extended nitrogen anneal at high temperature results in an increase in Q_{ss}.

There have been several models proposed to explain the nature of Q_{ss} but confirmation of its exact origin and mechanisms of its annealing are still unknown. In the unified model of Svensson (ref. 39) discussed

in Section III, the cause of Q_{ss} is the excess silicon centers near the interface, $Si^{\cdot}_{os}$ which become positively charged. This $Si^{\cdot}_{os}$ center is a silicon bonded to three oxygens within one or two monolayers of the interface. In Svensson's model, Q_{ss} is directly related to the amount of excess silicon near the interface. In the model of Maier (ref. 18), Q_{ss} is caused by an oxygen atom bonded to three interface silicon atoms, producing a donor with an energy level above the Si conduction band. Maier developed an equation relating the effective process-induced hole trap density to oxide thickness, temperature, oxygen partial pressure and oxide growth rate. The value of Q_{ss} after oxidation but before annealing is related to the rate of oxide growth. Thus in his conclusions, Maier suggests that the hole trap density is proportional to Q_{ss} immediately after oxidation.

Experimental investigation of the relation between Q_{ss} and hole trap density has never shown a correlation to exist. This is expected since it is known that a high temperature nitrogen anneal can reduce Q_{ss} but results in an increase in the hole trap density. However, in studies where the relation between Q_{ss} and hardness have been investigated, Q_{ss} was always measured at the end of the processing which usually included a post-oxidation anneal. The model discussed here predicts a correlation between hardness and Q_{ss} measured before the anneal. This implies an in-process test which would have to be performed on test wafers. The effectiveness of this technique has not been investigated. Therefore, verification is required. Since the technique involves in-process testing, it will be verified in phase II of this program.

d. Initial Interface State Density (N_{ss})

Because of the mismatch between the crystalline silicon and the stochiometric SiO_2 layer, defects occur at the interface having energy levels that lie within the silicon band gap. These surface recombination centers and traps occur both as acceptors and donors. The nature of these interface states and their density as a function of energy within the band gap has been the subject of extensive investigation. Many techniques have been devised to measure their energy density versus

position in the band gap. Most of the measurements have been performed on MOS capacitors utilizing C-V or G-V curves. Techniques developed to extract information about N_{ss} include high frequency (HF) C-V differentiation (ref. 54), comparison of low frequency (LF) or quasi-static (QS) C-V curves with ideal C-V curve (ref. 55), comparison of QS and HF curves (ref. 56), C-V curves at temperature extremes (ref. 57), deep level transient spectroscopy (ref. 58), and a-c conductance (ref. 35). Other techniques have involved Hall mobility measurements (ref. 59), and surface conductance measurements on MOS transistors (ref. 60). Many of these techniques involve a large volume of data and complicated data reduction schemes (refs. 35, 59) or measurements taken at temperature extremes (refs. 57, 60). The most commonly used and accurate method is the quasi-static (ref. 56). While this method is probably the most adaptable to use in a production environment (ref. 47), it is limited to looking at N_{ss} only over the center half of the band gap. The results of measurement techniques used to determine N_{ss} near the band edges (refs. 57-59) have yielded ambiguous results. Therefore, a clear picture of how N_{ss} varies across the entire band gap has not emerged.

Our knowledge of the origins of N_{ss} as well as the cause of the radiation induced increase in N_{ss} are similarly lacking. Several models have been discussed concerning the nature of both N_{ss} and the radiaton induced increase in N_{ss} (ΔN_{ss}). N_{ss} has been attributed to intrinsic bonding defects such as trivalent silicon, stretched bonds, and localization from randomly distributed charge. The radiation induced interface states, known to occur following hole transport to the interface, have been attributed to the release of hydrogen or hydroxyls which were involved in passifying interface bonding defects, or to charge localization from the additional trapped holes.

In addition to the questions concerning the origin and energy density of N_{ss} and ΔN_{ss} there are two additional confusion factors. First, with many techniques it is not clear whether the observed characteristics used to measure N_{ss} are actually due to N_{ss} or a result of

lateral nonuniformities (LNU) of trapped charge in the oxide. Because of this discrepancy, techniques have been developed to distinguish between N_{ss} and LNU's (refs. 61, 62). With much of the older data published on N_{ss} there is some question as to whether or not LNU's were present. Another problem in interpreting N_{ss} data is the ambiguity which prevents one from knowing whether the charged states are donors or acceptors. The generally accepted hypothesis is that the traps in the upper half of the band gap are acceptors and in the lower half, donors.

(1) Interface State Density in Mid-Gap

Although interface state generation from ionizing radiation has been studied rather extensively, no study was uncovered in which a conscientious effort was made to correlate the initial value of mid-gap N_{ss} to the radiation induced interface state density ΔN_{ss}.

All of the detailed studies of ΔN_{ss} have been aimed at characterizing the dose dependence of ΔN_{ss} for various oxide processing techniques and measuring its field, time, and temperature dependence.

One of the first studies in which N_{ss} and the postradiation value of N_{ss}, $N_{ss}(\gamma)$, were measured as a function of surface potential (ref. 63) concluded that for a given device, $N_{ss}(\gamma)$ was proportional to N_{ss} over the center half of the band gap. Measurements could not be made at the band edges in this study which utilized the QS-HF technique of Kuhn.

An analysis of the data presented in the study for mid-gap N_{ss} gave the results shown in Table 7.

These data indicate that the lower N_{ss} gives rise to a larger ΔN_{ss} which is consistent with the hydrogen passivation model discussed in Section III. However, the correlation is only reasonably high at one dose level and the sample size is quite small. Therefore, these tests do not give convincing support for the model, but certainly do not contradict it.

TABLE 7. DATA FROM SIVO ET AL. FOR UNDOPED OXIDES IRRADIATED WITH V_g = -10 V (REFERENCE 63)

N_{ss} ($\times 10^{11}/cm^2$)	ΔN_{ss} 10^5 rads ($\times 10^{11}/cm^2$)	ΔN_{ss} 3×10^5 rads ($\times 10^{11}/cm^2$)	ΔN_{ss} 10^6 rads ($\times 10^{11}/cm^2$)
1.17	4.01	6.12	17.83
1.67	3.55	4.65	15.33
1.08	2.08	4.91	11.32
1.62	0.85	4.53	10.78
1.29	1.38	4.62	11.61
2.47	0.71	3.81	11.3
Correlation Coefficient	-.48	-.75	-.29

If the data presented by Kjar and Nichols (ref. 64) are analyzed in a similar manner, no correlation is observed between N_{ss} (mid-band) and ΔN_{ss}. These data, however, were taken for many processing variations including chromium metallization and oxidation in the presence of HCl.

No general conclusions can be drawn from these studies concerning the correlation between N_{ss} (mid-gap) and ΔN_{ss}. Since the effectiveness of the technique has not been determined conclusively, it will be verified in this program. Mid-gap N_{ss} can be measured using either the QS-HF method or by measuring S_o on a gated diode. The use of gated diodes is being made more attractive for production assessment by the National Bureau of Standard (NBS). NBS is developing a gated diode structure which utilizes an on-chip FET amplifier. The output of this device will be a dc voltage proportional to the diode reverse leakage current. The amplification factor can be designed such that 1 volt will

correspond roughly to 1 pA current. Such a structure will lend itself to production wafer probe testing. It is anticipated that the device will be used in the present program to determine the effectiveness of using mid-gap N_{ss} as a screen for ΔN_{ss}.

(2) Interface State Density at the Band Edges

Very few studies have measured the radiation induced states near the band edges, primarily because of the difficulty in making such measurements. In a study by Whitefield and Southward (refs. 65, 66) the value of N_{ss} and ΔN_{ss} was determined at the band edges using specially designed micro-Hall devices. Their conclusion was that the value of N_{ss} within .1 to .15 E_V of the band edges can either increase or decrease with radiation. Data were taken on 25 devices in the study; however, data are presented on only two devices to demonstrate the variability. The data were taken on devices fabricated on n type <111> silicon substrates with a 700 Å dry gate oxide grown at 1000 C° with a 850 C° N_2 anneal. Figure 6 is a plot of the value of N_{ss} measured at the valance band edge, E_V, as a function of dose for the two devices discussed in reference 65. For the one device, N_{ss} decreases at $5X10^5$ rad(Si) then increases at 10^6 rad(Si). This peculiar behavior is attributed to competing mechanisms which affect edge states. No comparisons were made in this study between the initial value of N_{ss} at the band edge and the increase in Q_r. No other data could be identified in which measurements of edge state density were made before and after radiation.

The results of the experimental data discussed above do not indicate that the initial value of interface state density near the band edges can be used as a predictor for ΔN_{ss} or Q_r. However, consideration of the hole trapping model of Pepper would indicate that N_{ss} should be of some value as an indicator of hardness. As discussed in Section III the interface states near the band edges could be due to band tailing produced by the random fluctuation in surface potential from the dipoles trapped near the interface. If this is the case, a correlation should exist between ΔN_{ss} (E_C, E_V) and Q_r and N_{ss}(E_C, E_V) should decrease with radiation. However the data of Whitefield and Southward show an inconsistent decrease of N_{ss} (E_V) with radiation.

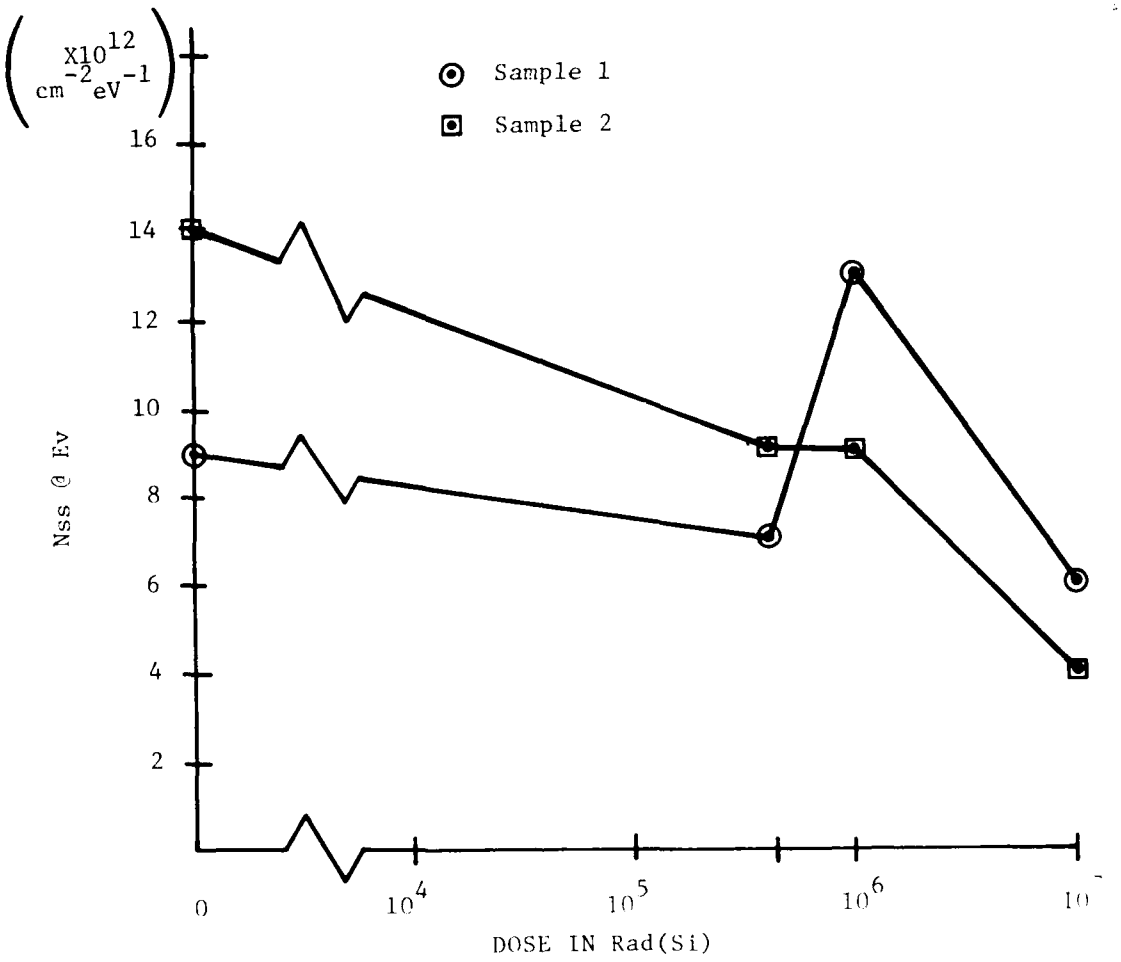

Figure 6. N_{ss} vs. Co^{60} Dose for N_{ss} at E_V (Reference 65)

In order to explore the predictions of the Pepper model, a practical method for measuring N_{ss} (E_V, E_C) must be found. Conventional room temperature measurements on MOS capacitors cannot be used since the surface potential cannot be swept out to the band edge in order to fill the surface states. The micro-Hall technique is not practical because of the amount of time required to acquire and reduce the necessary data.

Pulse techniques, such as constant capacitance DLTS, require both sophisticated equipment and data reduction techniques as well as low temperature measurements which are not compatible with production testing. Maier is investigating the possibility of extracting N_{ss} (E_V, E_C) by analyzing MOSFET transconductance versus frequency data using s parameter measurements. The rationale for this approach is that as the frequency is increased, fewer interface states contribute to the decrease in conductivity. Thus, transconductance should increase with increasing frequency as the states having a time constant corresponding to the signal frequency drop out.

The ideal method for measuring N_{ss} (E_V, E_C) would be to have a device in which the fermi level could be swept out to the band edges while maintaining the device in depletion. This can be done with the nonequilibrium MOS capacitor, or gated diode. This device was studied rather extensively by Grove and Fitzgerald (ref. 67) and the analysis later modified by Pierret (ref. 68). This structure has been used for studying bulk traps (ref. 69) in the silicon such as gold centers. Sigurd Wagner *, while at Bell Labs, investigated using this device for measuring interface states over the entire band gap. The work by Wagner was not completed and thus never published. We have pursued this method as a possible means of measuring $N_{ss}(E_V, E_C)$.

The nonequilibrium MOS capacitor consists of MOS capacitor with a diffused region under the periphery of the gate forming a p-n junction. By applying a reverse bias to the p-n junction, the device can be forced into deep depletion such that the majority carrier fermi level can be swept out to the band edge. A band diagram for a p substrate device is shown in Figure 7 for several bias conditions. Figures 7a and 7b show flat band and inversion conditions, respectively for the capacitor with the junction voltage $V_R = 0$. This is the same as for an equilibrium MOS capacitor.

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*NOTE: Private communication with Sigurd Wagner.

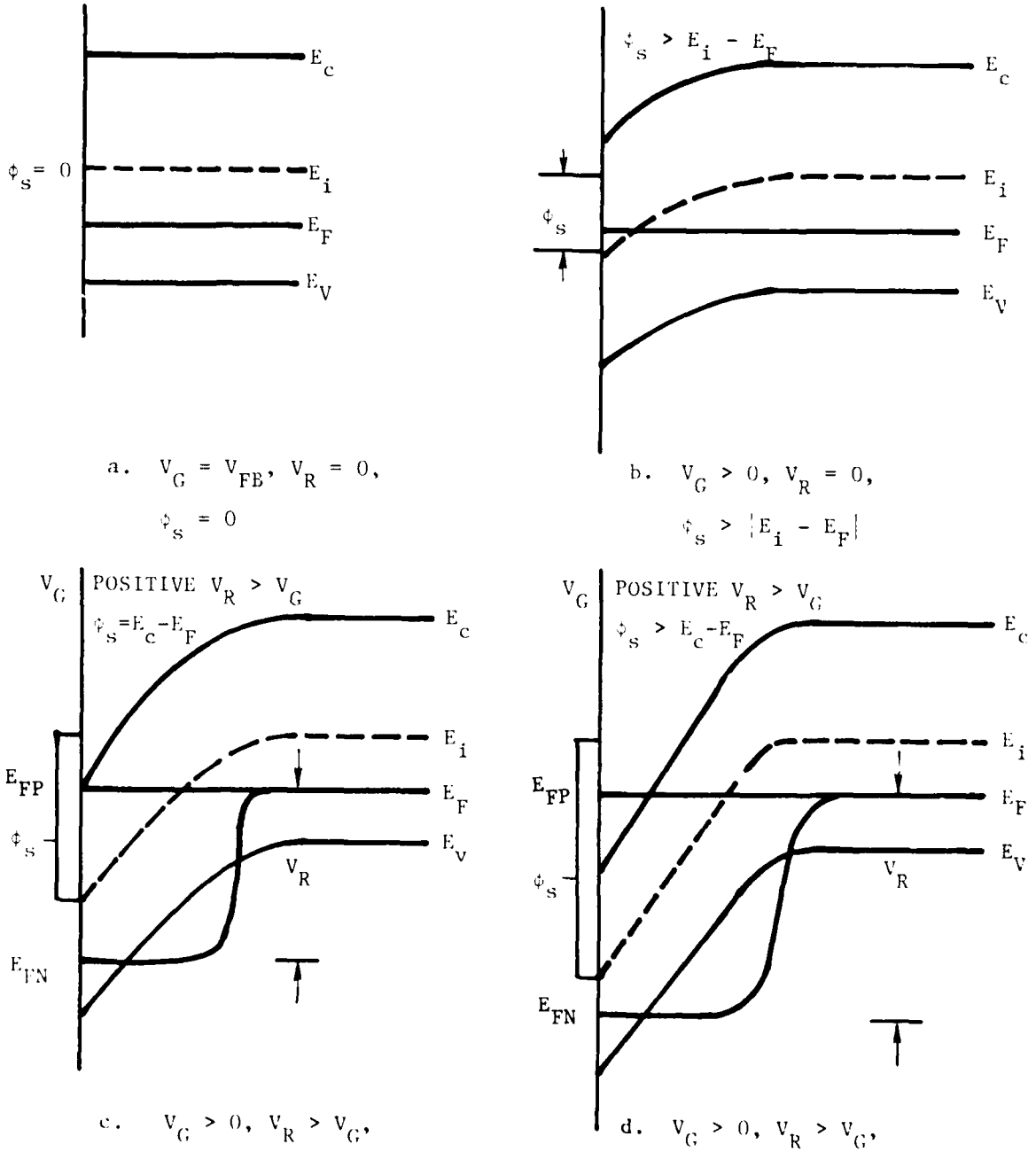

Figure 7. Band Diagram for p substrate Nonequilibrium MOS Capacitor

In Figure 7c, the surface potential has been increased to the point where E_F coincides with E_C. This is accomplished by applying a $V_R > V_G$ such that the quasi-fermi level for the minority carrier electrons is still in the lower half of the band gap, preventing an inversion layer from forming. If a large enough V_R is maintained, the majority carrier fermi level can be swept above the conduction band as shown in Figure 7d. Although this device conveniently allows one to move the majority carrier quasi-fermi level, E_{FP}, over the entire band gap, the minority carrier quasi-fermi level, E_{FN}, is still limited to the lower half of the band in order to maintain the depletion condition. This causes a problem in interpreting the data. All states above E_{FN} will be empty and all states below E_{FN} will have an electron in them. However, the states between E_{FP} and E_{FN} will be indeterminate, charging and discharging according to their characteristic time constants. It is these states which contribute to the reverse current component on the gated diode structure which is used to acertain the surface recombination velocity, S_o. Because of the ambiquities of the charge state for states located between the quasi fermi levels, it was decided that this structure was not appropriate for monitoring N_{ss} (E_V, E_C). However, since the device can be used for measuring a specific type of state, assuming all states are initially neutral and can only be charged one way, it will be used in the present program to investigate the density of donors in the upper half of the band gap and acceptors in the lower half. If these densities are small and decrease toward the band edges as expected, support will be given to the generally accepted but unproven assumption that the majority of states in the upper half of the gap are acceptors and the majority of the states in the lower half are donors.

In conclusion, no practical method for measuring edge states was found which could easily be implemented for production lot sampling. Therefore, no attempt will be made in the present program to correlate the initial value of edge state density with the radiation induced positive charge, Q_R. Verification of the Pepper diode model will be attempted through other parameters which relate to total oxide charge.

e. Total Oxide Charge (Dipoles)

The model for hole trapping based on the dipole theory of total charge in the oxide was discussed briefly in Section III. As mentioned, the idea that the oxide contains large numbers of both positive and negative charges was introduced by Nicollian, Goetzberger, and Heine (ref. 31) However, in their work, the charges were used to explain the origin of interface states and the correlation between the radiation induced trapped charge and increase in interface states. The work by Pepper (refs. 32, 70) is based on the concept of Anderson localization, whereby carriers in the inversion layer of a MOSFET can become trapped or localized in potential wells caused by random fluctuations in surface potential resulting from charges in the oxide near the interface. The localization has such a small activation energy that it becomes effective only when the fermi level is very near the band edge. This occurs below about 17 K; hence, all measurements made by Pepper were performed near liquid He temperature, 4.2 K. Because a much greater number of charges can be localized than the number of positive charges in the oxide, Pepper assumed that the total charge was much greater than the net positive charge, implying a large number of negative charges. The form of the charges proposed by Pepper is that of closely spaced pairs of positive and negative charges, or dipoles. He further proposes that about half the dipoles are within 40 Å of the interface where they can have a significant effect on the localization. The remaining dipoles are distributed in the oxide further from the interface. Additional justification for the dipole model of total charge is that the activation energy for carriers increases rapidly as the carriers approach the interface (under the influence of a substrate bias). This suggests a weak dipole potential rather than a simple coulombic potential. A possible model for the dipoles is suggested by Mott in the form of D+ and D- centers associated with nonbridging oxygens. Nonbridging oxygen centers in SiO_2 can be charged either positive or negative.

Experimentally, Pepper has measured the channel conductance versus gate voltage at very low carrier concentrations (weak inversion)

on p channel MOSFET's. He has found that at 4.2 K the conductance changes when carriers are first pulled away from the interface, then pushed closer to the interface by applying a substrate bias. Results of measurements on "hard" and "soft" devices are shown in Figure 8. What is observed is that for "hard" devices the conductance decreases slightly when the carriers are pushed closer to the interface and for "soft" devices, the conductance increases significantly when carriers approach the interface. This somewhat mysterious behavior is explained by Pepper in the following manner. In soft devices, the total number of dipoles is quite large. The potential fluctuations become large when carriers are further from the interface and thus decrease conductivity by localization When carriers are close to the interface, the wavelength is too small to allow localization. In hard devices the number of dipoles is much smaller

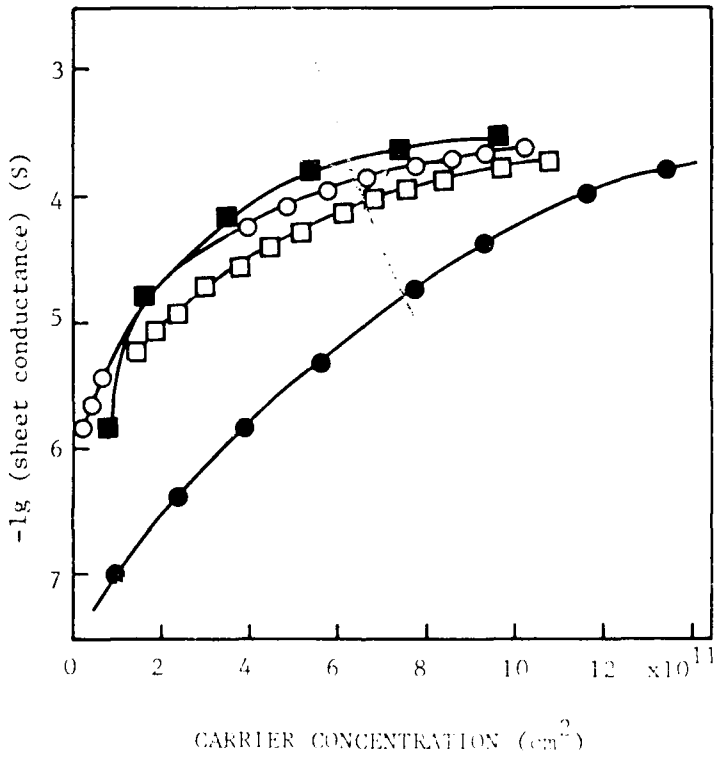

Figure 8. Conductance vs. Carrier Concentration (Gate Voltage) at 4.2 K. Solid Symbols Represent Soft Devices and Open Symbols Represent Hard Devices. Circles are Without Substrate Bias and Squares are for Substrate Bias Which Pushes Carriers Close to Interface. (Reference 32)

and so they are spread further apart. This allows each dipole to have a greater short range effect on the localization. The conductivity decreases in hard devices due to the localization when carriers are pushed near the interface. However, the decrease is small because there are fewer dipoles.

Pepper further proposes that upon irradiation, the negative center of the dipole acts as a hole trap. Thus, after irradation, the total number of dipoles decreases. This is verified by experiments on irradiated devices where he observes essentially one fewer dipole for each trapped hole.

Based on the data of Pepper, a 100 percent screen exists for MOSFET's in the form on conductivity versus carrier concentration with and without substrate bias at 4.2 K. The effectiveness of the screen has only been determined on two sets of p channel devices, one fabricated with the same process except for a high temperature (1000 °C) nitrogen anneal known to increase the hole trap density. In order to determine the effectiveness of this method as a prediction of hardness within a processing lot or from device type to device type, a much wider range of experimental data is required.

A major limitation of the method is the requirement of measurements at liquid He temperatures. Very few manufactures have cryogenic laboratories. In addition, even with a liquid He dewar, the number of devices that can be measured at one time is quite limited. Based on these considerations, the experimental method of Pepper is rejected as a production lot hardness assurance technique on the basis of practicality.

In order to implement the technique, a room temperature measure of dipole density is required. Most standard electrical measurements are not useful since they are only sensitive to net oxide charge. A possible solution is suggested by the work of Nicollian and Goetzberger (ref. 35) in which they attributed random potential fluctuation in the surface potential to the total charge in the oxide. In order to explain the broad peak of MOS capacitor gate to substrate ac conductance versus frequency, they assumed a dispersion of time constants due to fluctuations in the surface potential. After exploring other possibilities for

the cause of the potential fluctuations, such as a random distribution of ionized impurities in the silicon or random fluctuations in the oxide thickness, they determined that the potential fluctuations are due to the random distributions of fixed oxide charges and charged interface states. Therefore, if the total charge in the oxide is significantly larger than the net charge, it could be the dominant cause of the potential fluctuations. Nicollian and Goetzberger developed a relation between the standard deviation in ϕ_s and the total charge $\bar{Q}$ as follows.

$$\sigma_s = \frac{d(\bar{\phi}_s)\beta}{[d(\bar{\phi}_s)C_{ox} + \varepsilon_{si}]} \left(\frac{q\bar{Q}}{\alpha}\right)^{1/2}$$

where d is the depletion width, $\beta = \frac{q}{kT}$

C_{ox} the oxide capacitance, ε_{si} the silicon permitivity and α a characteristics area over which the surface potential, ϕ_s, is uniform. Assuming that the ϕ_s fluctuations are due only to the randomly distributed charges in the oxide, and at the interface, the dependence of conductance on frequency can be determined from the relation

$$\frac{G}{\omega} = \frac{q\ N_{ss}}{8\pi\ \sigma_s} \int_{-\infty}^{+\infty} e^{\left[-\phi_o + \phi_s - \phi_B + \frac{(\phi_s - \phi_s)^2}{2\phi_s^2}\right]} \ln(1+e^{2(\phi_o + d_s - \phi_B)})d\phi_s$$

Using this equation, an excellent fit to the experimental $\frac{G}{\omega}$ versus frequency curve was obtained using an α of $2.5\times10^{-10}cm^2$. Since the broadening of the experimental $\frac{G}{\omega}$ versus frequency curve is attributed to the time constant dispersion from ϕ_s fluctuations, one would expect a correlation between the total oxide charge, hence, dipole density, and the width of the ac conductance peak. In the present program, the technique of predicting hole trapping from ac conductance versus frequency curves will be verified on MOS capacitors.

Another technique for measuring the total oxide charge is suggested in the work of Nicollian and Melchior (ref. 36). In this paper, the authors suggest that the mean and standard deviation of the surface potential determines the frequency range over which MOS capacitor gate noise exhibits a 1/f dependence. The standard deviation of surface potential due to randomly distributed oxide and interface charges is the same as that used in the ac conductance discussion. They suggest that the value of σ_s can be experimentally determined from a plot of noise spectrum versus frequency as shown in Figure 9.

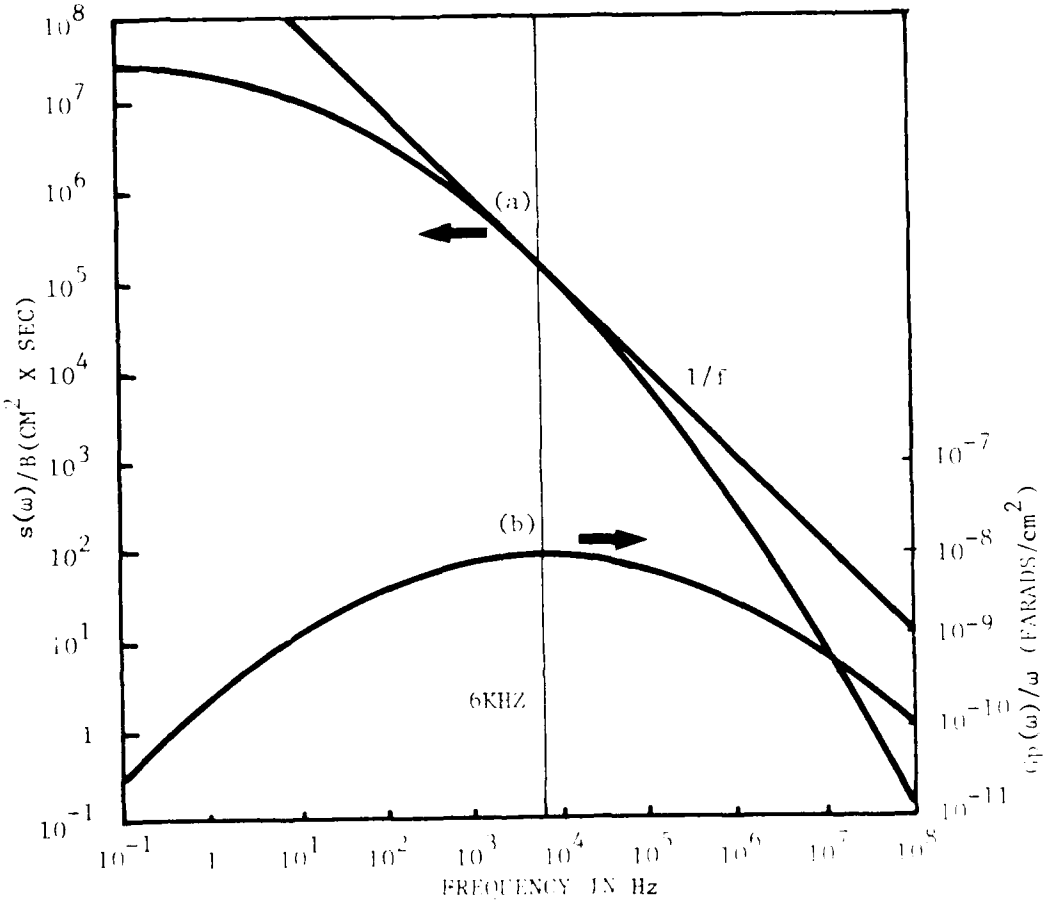

Figure 9. Curve (a) is a Log-Log Plot of $s(\omega)/B$ vs. Frequency and Curve (b) is a Log-Log Plot of $G_p(\omega)/\omega$ vs. Frequency. Both Curves are Calculated for a Standard Deviation of 2.6, a Hole Density at the Surface of 6.5×10^{12} cm^{-3}, a Hole Capture Probability of 2.2×10^{-3} cm/sec, and Interface State Density of 3×10^{11} $cm^{-2} xeV^{-1}$ and a Temperature of 300 °K (Reference 35)

The noise at very low frequencies is independent of frequency and thus approaches a constant. At high frequencies the noise spectrum tends toward a $1/f^2$ dependence. At intermediate frequencies, where the conductance is a maximum, the noise has a 1/f dependence. The standard deviation of surface potential, σ_s, can be determined from the relation

$$f_{H,L} = f_p e^{\pm(2\pi)^{1/2}\sigma_s}$$

where f_p is the center point frequency (frequency where conductance is a maximum), and $f_{H,L}$ are the high and low values of frequency where the experimental curve departs from the 1/f dependence. This experimentally determined value of σ_s should then be proportional to the total oxide charge, hence, hole trap density. The correlation between σ_s and total dose hardness will be examined in the verification phase of this program.

f. Stress at the Interface

Because of the mismatch between the thermal coefficients of expansion of SiO_2 and Si, a large stress exists at the interface at room temperature. The correlation between this stress and the fixed oxide charge density, Q_{ss} has been explored as a function of the oxidizing temperature (refs. 71-73). Using data from Deal et al. (ref. 17) for dry oxides, Lane (ref. 71) has shown an inverse relation between interfacial stress and Q_{ss}. Friedrich (ref. 72), on the other hand, presents data showing an increase in Q_{ss} with increasing interface stress. Brotherton et al. (ref. 73), in a systematic investigation of the relationship between Q_{ss} and stress, concluded that no consistent charge-stress correlation exists, and thus interfacial stress is not responsible for the presence of an interfacial charge.

No studies were found in which the relationship between oxide interface stress and radiation induced oxide charge, Qr, was investigated. However, a model has been proposed (ref. 25) in which the hole trap density in the oxide is attributed to a relaxation of the stress due to viscous shear flow at elevated temperatures. This model has been discussed in Section III. In an earlier report, Lane (ref. 74) suggested that stress relaxation gives rise to interface states which can degrade device performance. He did not, however, indicate a relation between stress relief and Qr.

The essence of the viscous shear flow model is that microscopic viscous flow occurs at the interface during oxidation cool-down and subsequent processing steps. This shear flow creates hole traps near the interface which can trap holes injected into, or created in the oxide. If this model is accepted, the hardness assurance task is directed towards a practical method of measuring the amount of viscous flow and hence, stress relief that occurs during oxidation cool-down and subsequent high temperature processing.

Several methods exist to measure stress in thermal oxides on silicon wafers. In the study by Botherton et al. (ref. 73), the stress was measured by the APEX x-ray diffraction technique (ref. 75). Friedrich measured wafer warpage by an interference technique (ref. 72). Lane (ref. 74) made measurements on a portion of the oxide which was overhanging the silicon. In the Lane method a window was formed in the oxide, then the silicon was etched away through the window. The undercutting which occurred caused a portion of the oxide to extend beyond the silicon edge. This overhang took on the shape of a wave whose characteristics were related to the stress. The method used by EerNisse (ref. 76) involved a measurement of the separation of two originally parallel laser beams. One beam was reflected off the clamped end of a cantilevered rectangular sample and the other reflected from the free end. The stress was related to the separation of the beams as compared to their separation from a standard reference flat-front surface mirror.

All of these techniques involve careful preparation of samples such as removal of any back surface oxide, and extreme precision and calibration. None of the techniques are easily amenable to production testing. In addition, the measurement of viscous shear flow during oxidation cool-down requires measurements in-situ in an oxidation furnace. This has only been accomplished with the laser beam method using a highly sophisticated setup. Another problem results in the required acccuracy of the measurements. EerNisse estimates the stress relief, as would be measured from a typical anneal cycle, to be .1 to 1 percent of the total stress. Thus, extreme precision is required to determine the actual amount of stress relief.

Based on these considerations, the measurement of stress relief as a screen for radiation induced oxide charge is rejected because of the difficulty in implementing the screen on a production line.

However, based on the recommendations of EerNisse (refs. 25, 76), certain processing guidelines should be implemented for radiation hardened MOS gate oxide processes. In all processing that occurs subsequent to the gate oxidation, temperatures above 925 °C should be avoided if times on the order of 20 minutes or greater are involved. The effects of temperature on viscous flow are illustrated in Figure 10 taken from reference 76.

3. PROCESSING PARAMETERS

The spacial distribution, density, and capture cross section of hole traps in the SiO_2 depends on many processing variables. In addition, the processing affects the initial as well as radiation-induced interface state density. The effects of processing on hardness for thermal SiO_2 layers on Si were first studied extensively by Aubuchon (ref. 13). After this initial work on pure SiO_2, efforts in radiation hardening took a different direction. Different insulators were studied, primarily Al_2O_3. In addition, oxides doped with various elements including Al and Cr were studied. Several years after the study by Aubuchon, however, work was again directed toward pure SiO_2. Derbenwick (refs. 14, 47) et al. at Sandia, performed a comperehensive study of the effects of processing variables on the radiation hardness of Al gate, thermal oxide CMOS devices. This study was followed by work at RCA (refs. 15, 28) to explore some of the dependencies noted in previous studies.

For bipolar devices, two studies were carried out to determine the effects of various bipolar processing variables on operational amplifier hardness. One study involved the LM108A (ref. 77) while the other utilized the μA741 (ref. 48) as the test vehicle. Both studies attempted to determine how the processing variables shown in MOS studies to be critical to hardness affected bipolar oxide hardness.

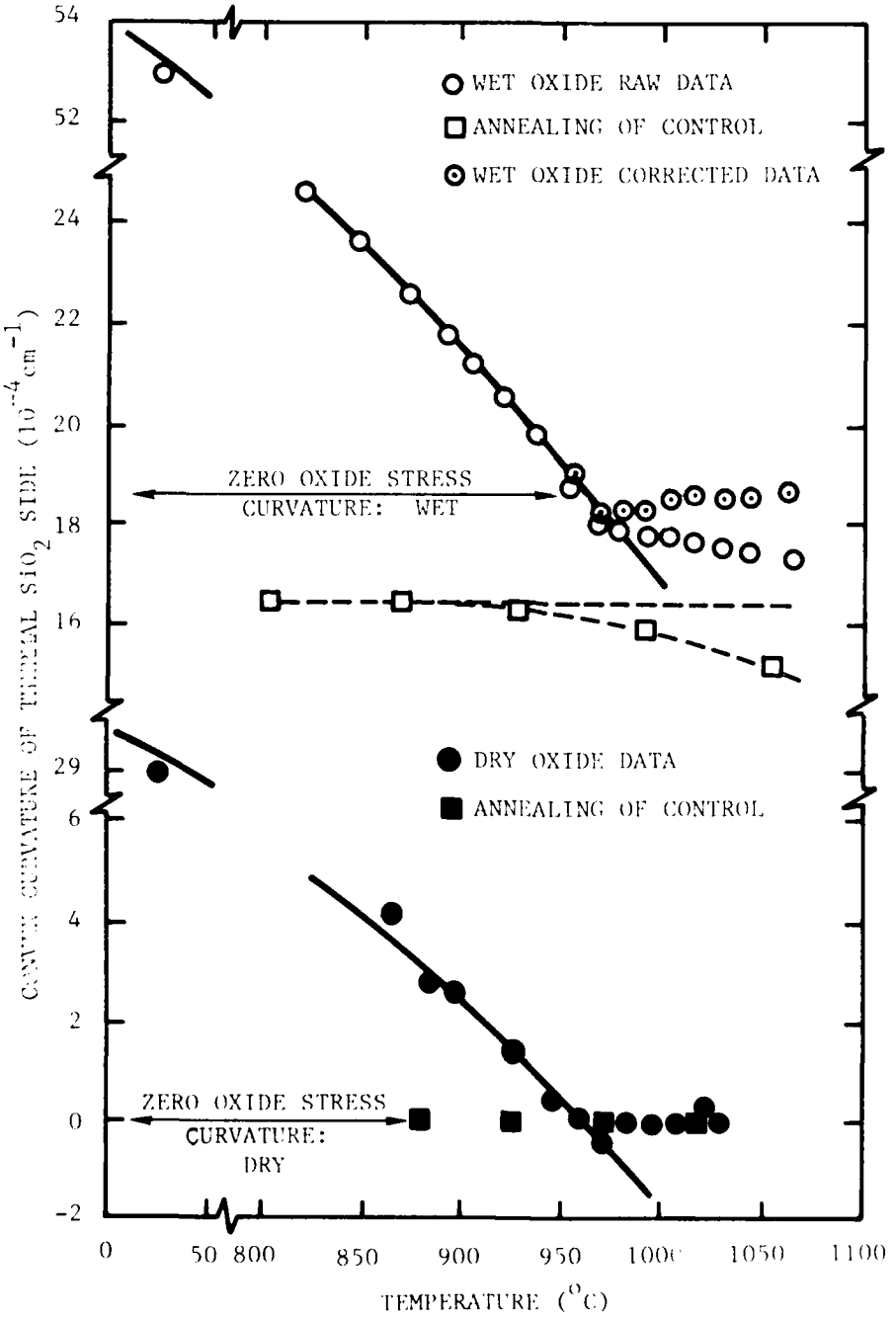

Figure 10. Measured Sample Curvature Versus Temperature for Si Samples with a Dry or Wet Oxide on One Surface. Controls are Samples with the Oxide Removed to Examine Residual Stresses in the Si Beneath the Oxide. Solid Lines are Thermal Warping Theoretical Results; Dashed Lines were Added for Viewing Purposes. (Reference 76)

a. MOS Processing

(1) Initial Silicon Surface Condition

The silicon surface condition has a significant influence on MOS device hardness. The reasons for this have been discussed rather extensively in the section on surface defects. Sandia (ref. 47) found that the variability in hardness could be significantly reduced by removing the top 1 μm of the as-received wafer. This can be accomplished by either growing a field oxide and stripping it or using an HCL vapor etch. The HCL vapor etch gave best results especially in terms of interface state generation. To avoid having to remove the top surface layer, the best approach is to obtain silicon wafers with extremely low surface defect density (less than 100 defects/cm^2). A screen can be placed on the as-received wafers to assure initial low defect density material.

(2) Pre-Oxidation Clean and Rinse and Photo-Resist

In the Sandia study (ref. 47), the pre-oxidation cleaning step was found to have a small effect on the hardness. Best results were obtained with a sulfuric acid clean followed by an HF dip. The deionized-water rinse did not affect hardness but lower resistance rinses ($\sim$1 MΩ), reduced the breakdown field in the oxide. The oxide breakdown field was also found to be affected by the photo-resist step. Although the hardness was unaffected, the oxide breakdown was lowered by use of one particular type of photo-resist, regardless of the chemical used to strip the resist.

Since the cleaning and photo-resist steps do not affect hardness to a great extent, no screens are necessary to indicate methods used in these processes.

(3) Oxidation Ambient and Crystal Orientation

All aspects of the oxidation growth process are critical to hardness including the crystal plane on which the oxide is grown. The amount of lattice mismatch between Si and SiO_2 is minimized and hence hardness maximized for the <100> plane, therefore almost all MOS processes utilize this orientation. The hardness is further dependent on the type of ambient (steam or dry O_2), the partial pressure, and the total time-temperature profile including the pull rate from the furnace.

The crystalline orientation of silicon greatly affects the interface properties with SiO_2 because of the nature and density of dangling bonds which occur at the silicon surface. The largest density is found for <111> and the smallest for <100>. Aubuchon (ref. 13) found that the radiation response of PMOS capacitors irradiated under negative bias was greatly affected by orientation, as shown in Figure 11. He attributed the difference in response as due primarily to a greater number of interface states generated in the <111> devices. Most of the work on radiation hardened MOS in recent years has been on <100> silicon. However, <111> is required for certain PMOS processing. In a study on <111> PMOS, Phillips (ref. 78) demonstrated an optimized hardened process, but the achievable hardness level was still below that of <100> silicon.

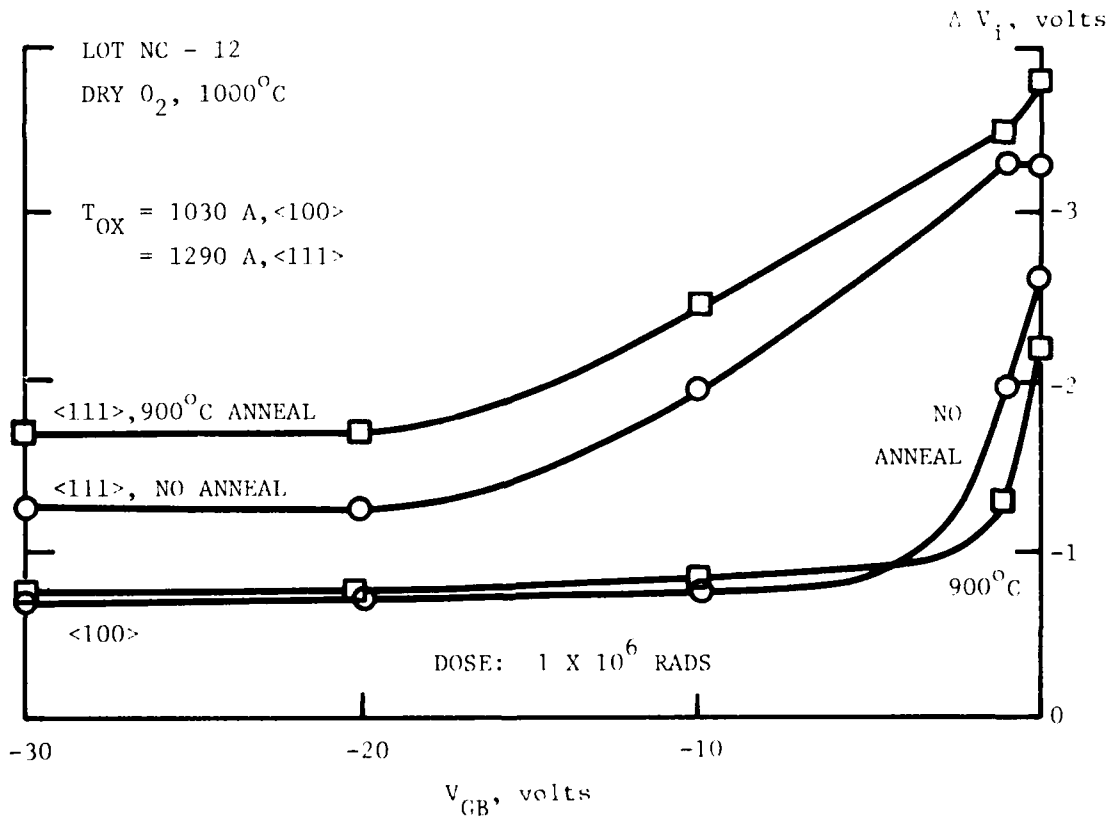

Figure 11. Dependence of the Radiation-Induced Voltage Shifts on Silicon Orientation for MOS Capacitors with Dry Oxides. (Reference 13)

The oxidation temperature has pronounced effect on radiation hardness. In the work at Sandia comparisons in ΔV_{FB} and ΔV_{TH} were made between six different lots of wafers grown in dry O_2 at different temperatures. The open and solid circles, squares, and triangles represent the spread in the data for the six different lots. The data, shown in Figure 12 were normalized to 700 Å using a t_{ox}^3 dependence. The results indicate that 1000 °C is optimum. Data taken by Hughes (ref. 28) at RCA indicate that the optimum temperature may lie between 900 and 1000 °C. The RCA data, shown in Figure 13, were normalized to 700 Å using a t_{ox}^2 dependence, and show only the change in V_{FB}. The results of these studies indicate that an optimum temperature for dry oxides exists, above or below which the hardness is degraded.

The hardness is significantly affected by whether the oxide is grown in a steam or dry ambient. The optimum process has been shown (refs. 13, 28) to be achieved with pure dry O_2 using HCL cleaned tubes. The difference between steam and dry oxides seems to involve not only the amount of H and/or OH incorporated at the interface, but a difference in the spacial distribution and capture cross sections of the hole traps (ref. 79). The hole trap density is larger in steam oxides and the centroid of trapped charge located further from the interface. Although the centroid of charge is the same for the same species of hole trap, in the steam oxides, there is an appreciable number of hole traps which are uniformly distributed in the oxide. This makes the effective centroid of trapped charge further from the interface. The time dependence of the interface state buildup after a radiation pulse is also quite different for steam and dry oxide (ref. 8). In steam oxides, the ΔN_{ss} increases slowly with time over several decades, whereas with dry oxides, ΔN_{ss} seems to appear nearly simultaneously with the hole trapping.

Based on these observations, there appears to be a significant difference in the structure of steam and dry oxides which affects hardness.

The effect of growth rate on hardness has been studied by Sandia by growing dry oxides in reduced partial pressures using nitrogen and argon as carriers. It was found that hardness decreases linearly

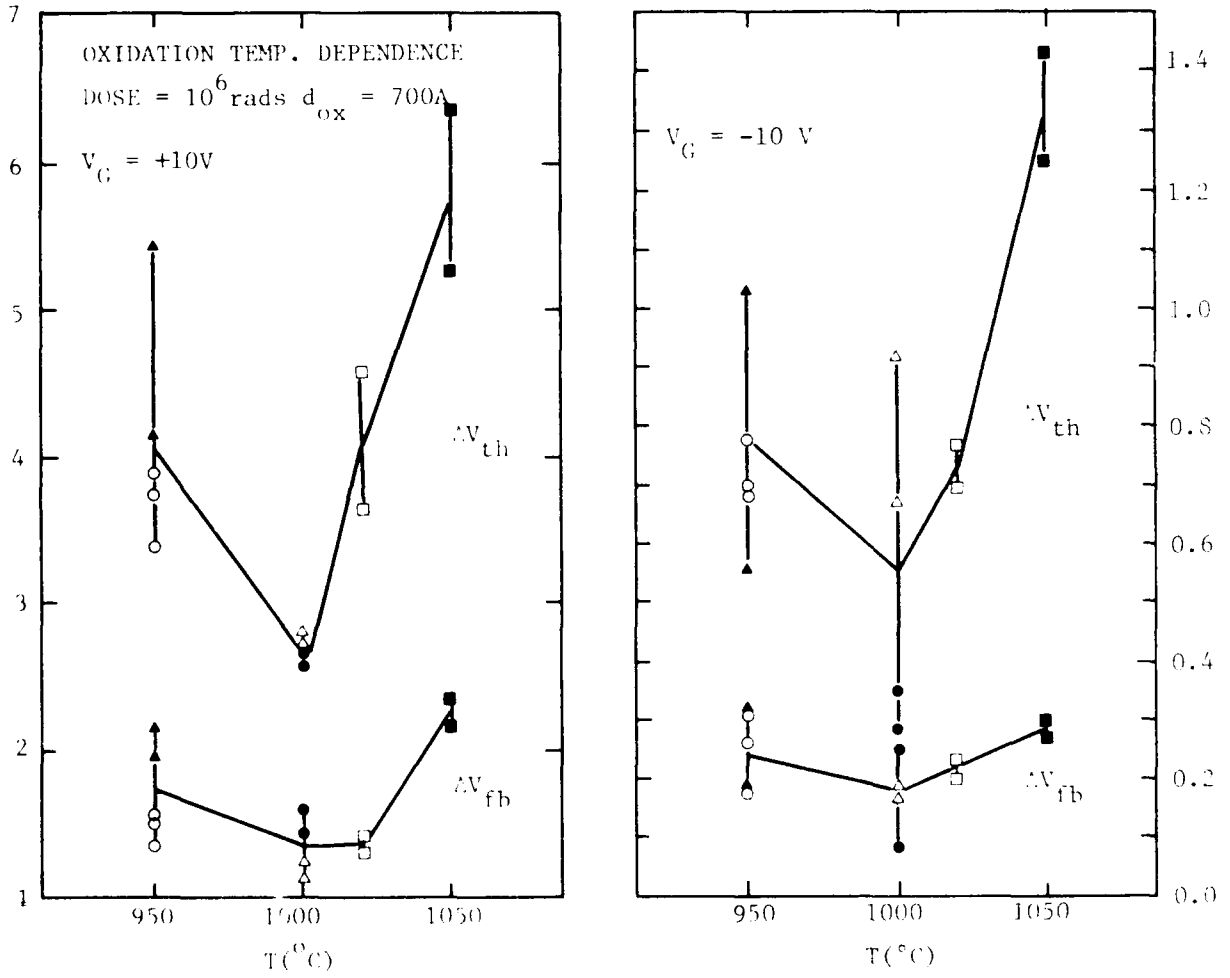

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Figure 12. Radiation-Induced Flatband and Threshold Voltage Shifts Versus Oxidation Temperature for Six Different Lots. (Reference 14)

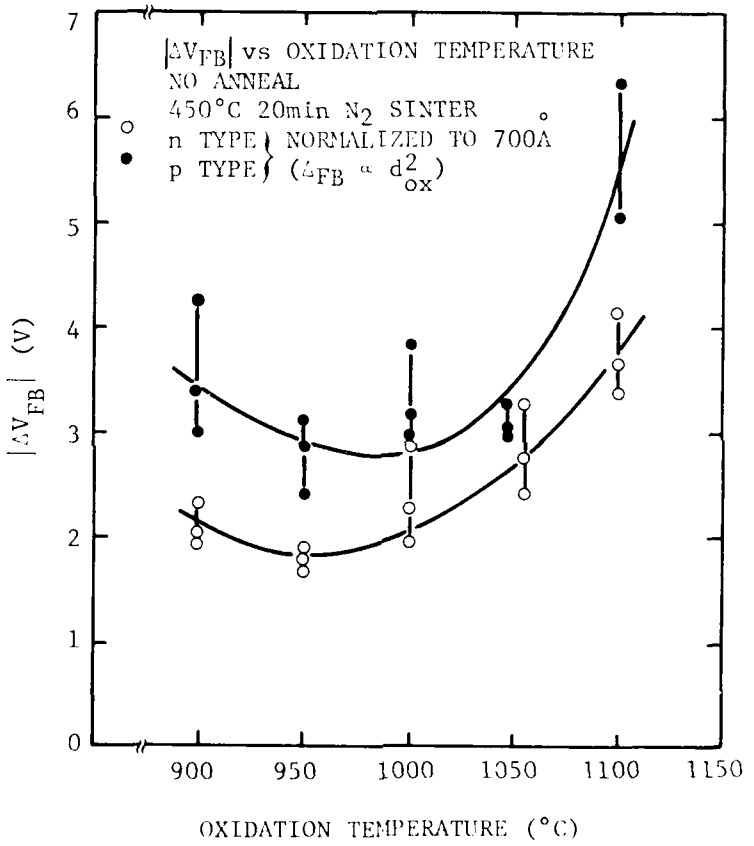

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Figure 13. Normalized Flatband Shift $|\Delta V_{FB}|$ Versus Oxidation Temperature for p- and n-type Silicon MOS Capacitors After Irradiation to a Total Dose of 10^6 rads. (Normalized to 700 Å using Square-Law Thickness Dependence.) (Reference 28)

with decreasing oxygen partial pressure when nitrogen is used. However, with argon, no effect is observed. It is assumed that the nitrogen causes additional hole traps in the oxide. From the measurements of the effects of these additional hole traps under both positive and negative bias, it has been deduced that the nitrogen-related hole traps are uniformly distributed in the oxide rather than being located primarily at the SiO_2-Si interface. The preirradiation C-V curves show no distinction between oxides grown in nitrogen and argon partial pressures.

(4) Postoxidation Annealing

High temperature anneals following gate oxidation almost always degrade hardness. Therefore, the ideal radiation hardened process does not utilize an anneal. However, the postoxidation anneal is useful for reducing Q_{ss}, which affects the initial value of V_{TH}. Sandia (ref. 47) has found that the effects on the radiation hardness of dry oxides can be minimized while still reducing Q_{ss} with an anneal of 825 °C for 90 minutes. No significant difference was observed between an argon and nitrogen anneal. Aubuchon (ref. 13) found that under negative bias irradiations, even an 800 °C N_2 anneal caused some degradation of the hardness of dry oxides whereas for steam oxides, the N_2 anneal improved the radiation response even above 900 °C.

(5) Metallization and Sintering

The type of metallization system has a definite effect on radiation hardness. Electron beam metallization processing, in which the aluminum (or other metal) is heated to the vapor stage by irradiating it with an electron beam, causes a degradation in the hardness, primarily for negative bias irradiations.

Galloway and Mayo (ref. 80) have shown that the x-rays given off by the electrons impinging on the aluminum can deposit up to 10^6 rad (Si) in the oxide during a typical metallization process. If additional hole traps are created near the SiO_2-Al interface by the x-rays, one would expect to see a larger effect on radiation response under negative bias than positive bias. Aubuchon (ref. 13) reported hardness degradaton on PMOS devices processed with e-beam metallization.

His data, shown in Figure 14, were taken under negative bias. Derbenwick (ref. 47) et al. reported that very little difference is observed in the hardness of e-beam versus induction heated aluminum under positive bias. However, significant degradation is observed for e-beam processed devices under negative bias. The degradation in hardness for e-beam systems using chromium rather than aluminum are not nearly as pronounced because (ref. 78): (1) less e-beam energy (hence fewer x-rays) is required to evaporate a given thickness of chromium; and (2) the chromium layer being deposited is a better shield against the x-rays than Al since its atomic number is higher.

For non e-beam metal systems, the induction (rf) heated crucible sources are preferred over a tungsten filament-evaporated metal system because of the lower mobile-contamination levels achievable.

For e-beam metallization, a postmetallization sinter is required to remove the x-ray induced degradation, although the sinter apparently does not anneal the additional radiation induced hole traps. However, even for non e-beam metal systems the hardness is affected by a sinter. Hughes (ref. 28) has studied the optimum sintering temperature and time for an N_2 sinter on induction-heated Al metal devices. His results indicate optimum hardness of both p and n type devices for a 450 °C, 40-minute sinter. In the Sandia study, it was found that N_2 sinters not only reduced the initial mid-gap N_{ss} but also possibly ΔN_{ss}. Hydrogen or forming gas sinters, however, were found to seriously degrade hardness, due to the incorporation of H at the interface.

Almost all of the major variables in MOS processing have been systematically investigated to determine optimum processing for radiation hardness. Unfortunately, virtually no tests can be run on a finished MOS circuit or even test devices (MOS capacitor or transistors) to determine how the device was processed. The results of the hardening studies can be used as guidelines for processing radiation hardened devices, or they can even be written down as process controls to be implemented by the maufacturer. However, a set of preirradiation tests on finished products cannot be defined to assure the user that the process controls have been adhered to.

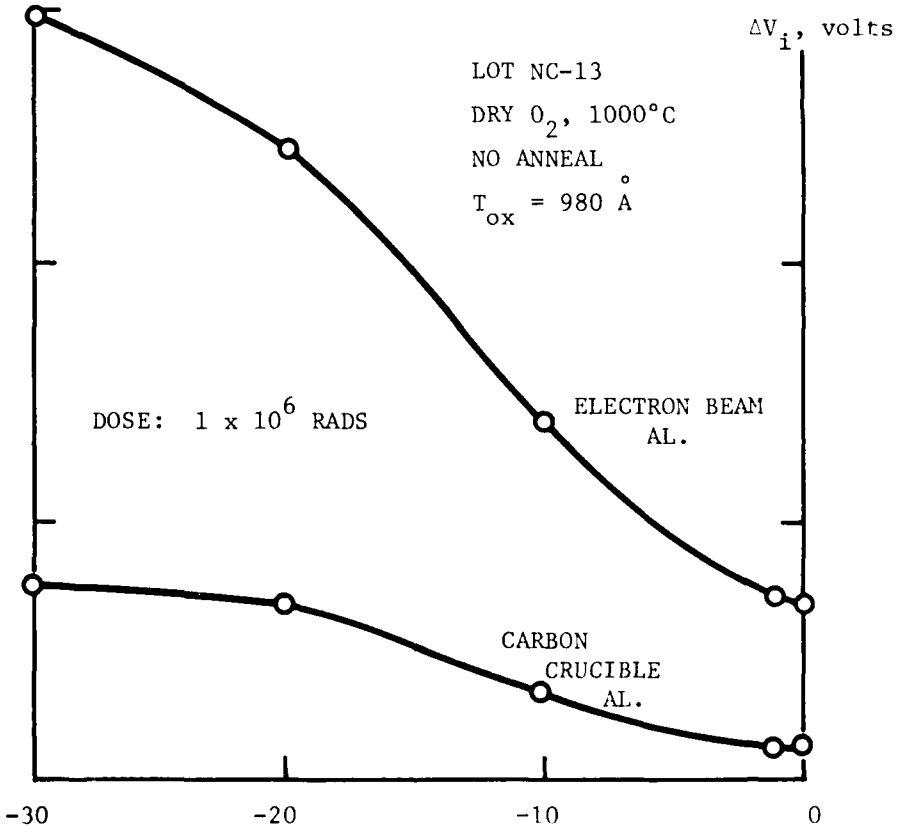

Figure 14. Radiation-Induced Shifts for Dry Oxide MOS Capacitors with Electron Beam-Evaporated Aluminum Gates as Compared with Aluminum Evaporated from a Resistance-Heated Carbon Crucible **(Reference 13)**

This makes the hardness assurance task quite difficult in terms of process control. Once can prescribe to a manufacturer that he:

(1) Use <100> silicon wafers with a surface defect density <100/ cm^2.

(2) Clean the surface with sulfuric acid, dip in HF and rinse with 18 MΩ water.

(3) Grow a 700 Å gate oxide in dry O_2 (< 10ppm H_2O) at 1000 °C in an HCl cleaned furnace.

(4) Anneal in N_2 at 825 °C for 90 minutes.

(5) Use low contamination induction-heated metallization and sinter in N_2 at 450 °C for 40 minutes.

(6) Use an inert gas during sealing.

The only known tests that could be applied to either a test device or circuit to verify that the above schedule had been adhered to are:

(1) Measure the gate oxide thickness.

(2) Measure the index of refraction of the oxide to determine whether it was steam or dry.

(3) Determine the crystal orientation of the silicon.

(4) Measure the type and density of impurities in the oxide.

(5) Measure the initial mid-gap interface state density to possibly detect a hydrogen anneal or sinter.

Items 1, 4, and 5 have been previously discussed in regard to surface and oxide properties (Subsection B). Determination of crystal orientation and oxide growth technique can be implemented but do not, of course, constitute screens in themselves. The only way such information could be incorporated into a screen would be to derive an empirical formula based on a specific process in which hardness was related to all of the critical processes. Then such variables as impurity content, surface defect density, t_{ox}, Q_{ss}, N_{ss}, crystal orientation, and index of refraction could be plugged into the formula to predict the ΔV_{TH} for that process. Such an approach, even if it were shown to be effective would not be practical since it would involve too many tests. A simple radiation sample test would be more cost effective.

The one item which can be easily monitored which not only affects hardness but is an excellent process control monitor is oxide thickness. Since the oxide thickness is very sensitive to crystal orientation, oxidation temperature and time, oxidation ambient, and oxygen partial pressure, it serves as a monitor of variations in any of these parameters. If the oxide thickness, whose nominal value is known for a given process, is off by as much as 10 percent, something has gone wrong in the process and the lot should probably be rejected due to an uncontrolled process variable. The dependence of hardness, usually measured by ΔV_{FB} on MOS capacitors, on oxide thickness has been studied rather extensively (refs. 28, 47, 48). The generally accepted relationship between hardness and oxide thickness, t_{ox}, is that for t_{ox} <1000 Å hardness is proportional to t_{ox}^3, for 1000 Å < t_{ox} < 10,000 Å, hardness goes as t_{ox}^2 and for t_{ox} > 10,000 Å hardness goes as t_{ox}.

In the studies at Sandia (ref. 47) over many processing lots, a t_{ox}^3 dependence was measured for the range of 400 Å - 1000 Å. This has been confirmed at several vendor facilities including Harris and National. In a study on bipolar oxides by Brown (ref. 48) a t_{ox}^2 dependence was measured on oxides between 800 and 8,000 Å. G. Hughes[32] on the other hand reports a t_{ox}^2 dependence for thin oxides (t_{ox} < 1000 Å). This dependence has not been confirmed on other hard thin oxides. Regardless of the exact dependence of ΔV_{FB} on t_{ox}, hardness is clearly a function of oxide thickness. One of these dependencies comes simply from the linear dependence on t_{ox} of the number of holes generated in a given volume of oxide with a given cross sectional area. Another t_{ox} dependence comes from the integration of the electronic field over the thickness to derive voltage. The third t_{ox} dependence is suppported by the viscous shear flow model of EerNisse and Derbenwick (ref. 25). A t_{ox}^3 dependence also results if one assumes that the centroid of the distribution of hole traps in the oxide is proportional to t_{ox}.

Within a given processing lot, the variations in oxide thickness, both across a wafer and from wafer to wafer, are very small. Therefore, as a screen for hardness, t_{ox} would be very poor. However, since t_{ox} is an excellent process control monitor, it will be evaluated as such in phase II of this program.

b. Bipolar Processing.

Many of the variables which affect MOS gate oxide hardening are also important in bipolar processing. However, bipolar oxides see many processing steps; for which very little latitude exists in altering their formation. Bipolar oxides are formed as a result of certain processing steps, they are not formed as a primary element of the device. Therefore, fewer processing steps can be significantly altered to harden bipolar oxides. Consequently the achievable hardness levels for bipolar oxides are much lower than for MOS gate oxide (most obviously because they are much thicker). Thus many of the variables which affect the hardness of gate oxides are second order effects in bipolar oxides. The total dose hardness of linear bipolar circuits is affected by both circuit design and the hardness of the SiO_2 and SiO_2 interface. Because of the strong field dependence of hole trapping and interface state generation, SiO_2 regions having a large positive field during radiation will experience much greater degradation. In linear circuits, where typical supply voltages run $\pm$ 15 V, various regions of SiO_2 above p-n junctions can see a potential of as much as 30 V if a metallization strip at +15 V crosses over a region biased at -15 V. Other regions of the op amp can see large negative fields in the oxide which would minimize hole trapping. The large differences in degradation which could result for different transistors in the circuit could cause an imbalance leading to early failure. Therefore much can be done to minimize the total dose effects in linear circuits by properly designing the metallization runs, such that critical components do not have large positive electric fields in the oxides above them. Proper design changes alone can significantly increase the total dose failure level of the circuit.

There have been two studies (refs. 48, 77) to investigate the process variations which affect the hardness of bipolar oxides on linear circuits. In a study (ref. 77) on the LM108A low power op amps, the failure modes were excessive leakage from collector to substrate for npn devices, from base to substrate for pnp devices and degradation of super β gain on the input transistors. The portions of the process investigated

were the oxide etch, phosphorous etch, and CVD densification in the double emitter formation, final anneals, metallization and glassivication. The results of this study are given in Table 8 taken from reference 77. The study found that stripping the thick isolation diffusion oxide improved hardness. For stability, phosphorous gettering seems to be necessary. Total removal of the P-getter did not improve hardness significantly. After the emitter deposition and drive, a deposited oxide is laid down. The process used to densify this oxide was studied. Best results were obtained with steam. Any oxide densification gave poor results.

TABLE 8. SUMMARY OF RESULTS OBTAINED FOR PROCESS MODIFICATIONS (REFERENCE 77)

PROCESS STEP	RADIATION SENSITIVITY	COMMENT
ISOLATION OXIDE ETCH	SIGNIFICANT IMPROVEMENT WHEN ISOLATION OXIDE REMOVED	CARE NEEDED TO PREVENT FIELD INVERSION
PHOSPHOROUS ETCHED DURING EMITTER FORMATION	MINOR IMPROVEMENT WHEN ALL P_2O_5 GLASS REMOVED	NOT VIABLE DUE TO T/B PROBLEMS
DENSIFICATION OF CVD OXIDE (EMITTER) (OXIDIZING AMBIENT)	A. HCL STEAM VS STEAM (CLEAN FURNACE) MINOR IMPROVEMENT WHEN HCL REMOVED	YIELD POOR WITH DRY OXIDE-CONTACT PROBLEMS
	B. WET VS DRY O_2 SIGNIFICANT IMPROVEMENT FOR WET	LARGE N_{SS} INCREASE WITH DRY O_2 ANNEAL
EMITTER OXIDATION ANNEAL AND POST EMITTER ANNEALS	SIGNIFICANT IMPROVEMENT BY REPLACING FORMING GAS WITH DRY NITROGEN	NO IMPACT ON YIELD NOTED

PROCESS STEP	RADIATION SENSITIVITY	COMMENT

TABLE 8. SUMMARY OF RESULTS OBTAINED FOR PROCESS MODIFICATIONS (REFERENCE 77) (Concluded)

PROCESS STEP	RADIATION SENSITIVITY	COMMENT
METALLIZATION	A. SIGNIFICANT IMPROVEMENT WHEN METAL OVERLAY IS USED OVER THE E-B JUNCTION OF AMP TRANSISTORS	METAL MASK CHANGE NEEDED
	B. FILAMENT, E-GUN AND RF HEATED SOURCE: 2D ORDER EFFECT IN IMPROVEMENT: RF METAL PREFERRED	
GLASSIFICATION	SIGNIFICANT IMPROVEMENT WHEN P-DOPING IS REDUCED	CARE NEEDED TO MAINTAIN STEP COVERAGE
PACKAGING	DEPENDENT ON VENDOR-FLATPACK CAN BE WORSE	

The use of forming gas both in the densification and anneals was studied. Better results were always obtained when forming gas was removed. Significant hardness was observed when a metal overlay was applied above the E-B junction of all transistors. No measureable difference was observed between e-beam metal and induction heated metal, in contrast to MOS results. Non-doped glassification gave better results than the standard variable doped glass. For these devices no effect was seen from packaging.

In the other study (ref. 48) μA741 processing was used as the baseline for investigation. All measurements to determine the effects of process variations were made on MOS capacitors. All silicon wafers for the study came from a single crystal.

The following conclusions were reached from the study:

(1) Mobile-ion contamination. No correlation was observed between hardness and mobile-ion density for $Q_{ION} \geq 5 \times 10^{11}/cm^2$.

(2) Location of wafer in crystal. No effect on hardness.

(3) Preparation of silicon surface. No effect on hardness even though the preparation technique had a significant effect on surface defect density.

(4) Oxidation ambient. No significant difference between steam and dry oxides. The differences depended mainly on how they were annealed. Dry or steam were hardest if cooled in dry O_2 rather than annealed in N_2 at oxidation temperature. A postoxidation dry O_2 was sufficient for increasing hardness.

(5) Oxidation thickness. ΔV_{FB} was found to be proportional to t_{ox}^2 from 600 - 6000Å.

(6) Metallization. No difference between e-beam and induction heated sources.

(7) Surface defect density. No correlation between hardness and process induced defect density was observed either from wafer to wafer or across a wafer.

(8) High temperature diffusions. The hardness was significantly lowered by the boron diffusion cycles used for isolation and base processes, but not by the phosphorus diffusion used for emitters. However, the hardness lost by the boron diffusion was in part regained by subsequent processing.

The general conclusion that can be drawn from these two studies is that bipolar oxides are exposed to many more processing steps than MOS gate oxides which affect their hardness. They are subjected to higher temperatures for longer times, they are much thicker, they are usually grown on <111> silicon, and they have a much higher potential for contamination. With every device the process is different so a new set of variables has to be considered. This makes the hardness assurance task even more difficult for bipolar than MOS in terms of process controls. A different set of process controls would probably be necessary for each linear bipolar process in order to achieve uniform hardness. As was shown in the two studies, several processing steps which are critical to MOS hardness are second-order in bipolar devices. Also, many processing steps which are first order in bipolar processes do not even exist in MOS processes.

Therefore, if process controls are to be considered for total dose hardness assurance of bipolar devices, a complete study would be in order for every unique device to identify the critical processing steps.

4. HOLE INJECTION TECHNIQUES

If our current understanding of hole trapping and interface state generation phenomena is correct, then in order to induce "total dose" effects in semiconductor devices, one does not have to irradiate the device but merely provide a source of holes to the SiO_2 layer. Carrier injection into the SiO_2 has been used both for studying hole trapping and, by injecting electrons, trapped hole depopulation. Almost all of the carrier injection techniques have been used to study basic mechanisms such as energy levels associated with hole traps, the spacial distribution of hole traps and their capture cross sections. However, very few studies have investigated the use of carrier injection techniques as a substitute for a radiation test. The desirability of such a substitute radiation test would be in terms of cost, implementation, and the additional information that might come from the injection technique. The first requirement for a substitute radiation test is, of course, to establish correlation between the changes in electrical parameters resulting from the hole injection and the changes resulting from a radiation test. To our knowledge, this correlation has only been studied for two of the charge injection techniques (refs. 10, 28).

Hole injection techniques which show some promise of success as a hardness assurance subsitute for a radiation test are:

(1) Corona discharge.

(2) p-n junction avalanche.

(3) Bulk avalanche.

(4) Negative bias temperature stress.

Photo injection techniques do not appear to work for hole injection.

Each of the four hole injection techniques will be considered in terms of effectiveness and practicality.

a. Corona Discharge

One method of creating positive trapped charge in SiO_2 similar to that caused by irradiation, is to charge the free surface of the oxide with a negative corona in air (ref. 81). A corona tip is charged to about -12 kV forming negative ions (thought to be CO_3-) which are thermalized and transported to the oxide surface. A large field builds up in the oxide which attains a steady state value of about 14 MV/cm. This steady state value is reached when the current through the oxide equals the ionic current from the corona tip. Woods and Williams (ref. 81) have proposed several charging mechanisms for the positive charge left in the oxide. The most likely mechanism is tunneling of an electron from a neutral hole trap in the SiO_2 into the SiO_2 conduction band. The electron is then transported to the silicon under the influence of the large negative field. Other less likely processes involve hole-electron pair production by hot electron impact ionization and direct tunneling of a hole from the silicon conduction band to the trap in the SiO_2.

Etch-off experiments on negative corona charged oxides indicate that nearly all the trapped positivie charge is near the SiO_2-Si interface with a centroid of about 130 Å. Prolonged charging of the surface of greater than 2 minutes does not increase the value of trapped charge but does create a distortion and pronounced hysteresis of the C-V curves. This is likely due to the creation of fast surface states.

Although no detailed correlation studies have been done between corona charging and radiation charging, a study by G.W. Hughes (ref. 28) provides qualitative data. In an experiment to determine the effect of metallization and sintering on the hardness of thermal oxides, flat band voltage shifts (ΔV_{FB}) from corona discharge were compared to ΔV_{FB} values from 10^6 rad(Si) Co^{60} irradiations. In order to charge an oxide with the corona discharge method, no metallization is required. Therefore, in-process charging of unmetallized oxides can be performed. C-V curves are made with mercury probes. In the experiment by Hughes, several wafers were characterized by negative corona on one half the wafer. The other half received metallization and sintering and was tested in a Co^{60} source.

Comparison of the ΔV_{FB}'s between corona discharge and Co^{60} is given in Figure 15 for six wafers. The results show very good qualitative agreement for the two methods, and further indicate that the metallization and sintering process apparently does not affect the hardness of the oxides.

The data of Woods and Williams (ref. 81) indicate that the charging of the oxide from negative corona is very similar in nature to that from radiation effects. The spacial distribution of trapped holes after corona discharge implies that the same hole traps are being filled as with radiation and the prolonged corona experiment indicates a subsequent buildup of interface states. The data by Hughes provide additional support for the correlation between corona and radiation charging. Based on these data, the negative corona discharge technique appears to be an effective hardness assurance technique which can be applied in process as a diffusion lot wafer sample test. One or two test wafers could be pulled after gate oxidation and subsequent annealing and subjected to a negative corona for sufficient time to induce an equilibrium value of SiO_2 charging. The wafers would then be characterized for flat band voltage shift using mercury probes. Lots passing the wafer sample test would continue through metallization, sintering, and packaging. The advantages of such a technique would be a large cost savings by in-process lot qualification, thus avoiding expensive packaging and testing of unqualified devices. The disadvantage is the requirement for highly specialized equipment which has not been developed for production line usage. In order to use the technique, corona discharge equipment and mercury probes are required. Because of the potential for contamination with the use of the mercury probes, the sample testing would have to be done on expendable wafers, such as pilot wafers.

Although the data are somewhat limited, the corona discharge method appears to be an effective diffusion lot screen for hardness. However, the implementation of the method severely limits its use as a production screen. Because the subcontractor chosen for this program does not possess the necessary equipment, this technique will not be evaluated in a production environment.

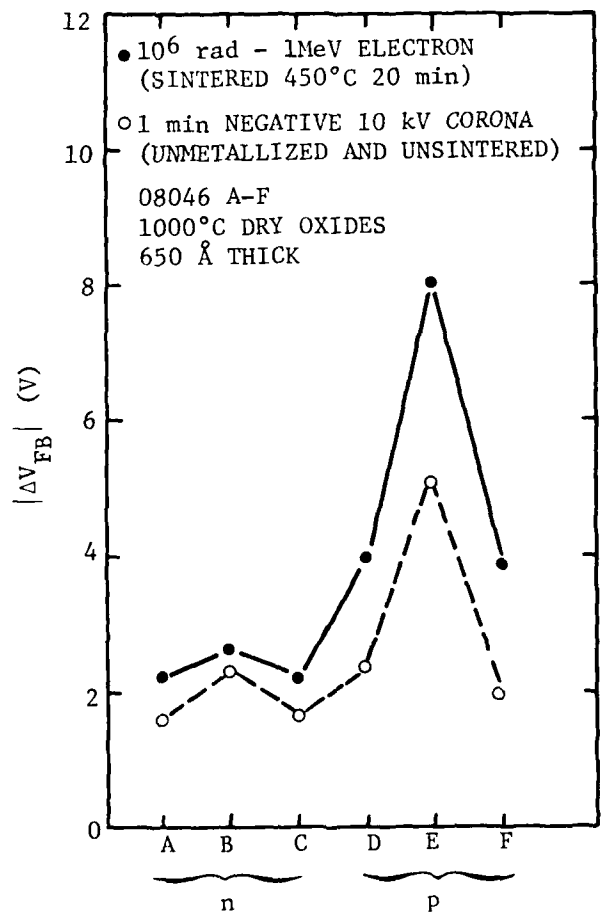

Figure 15. Flatband Shift $|\Delta V_{FB}|$ Displayed for Six Different Wafers in an Irreproducible Run. Solid Dots are for 1 MeV Electron Irradiation of 10^6 rads Total Dose. Open Circles are for Negative Corona-Charged Oxides. (Reference 28)

b. p-n Junction Avalanche Techniques

If a p-n junction is reversed biased to the point of avalanche, the carriers in the avalanche plasma attain considerable energy. Hot carriers in the plasma near an $Si-SiO_2$ interface can surmount the barrier height and enter the oxide. If a large negative electric field is present in the oxide, hole injection becomes dominant over electron injection. These concepts have been applied in both bipolar and MOS transistors to create hole trapping and interface state generation. Although no studies were identified in which the damage due to p-n junction avalanche hole injection were correlated to radiation damage, several studies have characterized the nature of the damage in both MOS and bipolar devices due to avalanched junctions.

1) Bipolar Studies

It has long been known that avalanching the E-B junction of a bipolar transistor can cause degradation of h_{FE}, especially at low currents. Several studies (refs. 82-85) have sought to explain this degradation. Collins (ref. 82) investigated the degradation mechanisms by stressing the reversed biased E-B junctions of npn devices at breakdown currents between 1 μA and 10 μA for both pulsed and steady state conditions. He performed studies on both normal and field-plated devices although all of the stressing was done with a field plate voltage of zero volts. He found that the gain degradation, as measured by $\Delta I_B/I_{BO}$, where ΔI_B is the stress induced change in base current at constant collector current and I_{BO} the prestressed base current, increased with both the stress time for a constant stress current, and stress current for a constant time. However, $\Delta I_B/I_{BO}$ did not change appreciably with temperature. He attributed the degradation to an increase in base surface recombination velocity from the creation of fast interface states, rather than due to an ionic drift. However, Colins found that not all transistors degraded from E-B stressing. In a few device types, the h_{FE} actually increased after stress.

In a more comprehensive study, McDonald (ref. 83) studied the change in the I_B versus V_G characteristics as a function of stressing under positive, negative and zero gate bias. The gated devices used by

McDonald were specially designed and prescreened for low mobile ion content. Under zero gate bias, the base current versus V_G at a fixed V_{BE} developed a peak near V_G=0 as shown in Figure 16. This peak increased with the stress time at a constant current. The peak was explained in terms of the spacial location of the surface states induced by the stress. If the avalanche plasma is confined to a small region on either side of the metallurgical E-B junction at the interface, then the interface states are also confined to this narrow region. In the measurement of I_B versus V_G the metallugical E-B junction moves laterally along the base surface and away from the location of the stress-induced surface states. This is shown in Figure 17. For a negative gate voltage, the n+ emitter is depleted and the p base is accumulated which moves the intrinsic point toward the emitter. For a positive gate voltage, the opposite occurs and the intrinsic point moves into the base. Since the maximum recombination rate occurs at the intrinsic point, the base surface recombination current decreases as the intrinsic point moves further from the spacial location of the stress-induced surface states. This gives the characteristic hump at V_G=0.

McDonald calculated the width of this hump as a function of base doping, emitter diffusion parameters, and the spacial distribution of surface states. His calculations explain why Collins did not see a hump in his data, since for the devices used by Collins, the hump would have a V_G width of about 200 volts.

Stress under a negative gate voltage results in a hump in the post-stressed I_B versus V_G curve which is displaced toward negative voltage. This is explained in part by the fact that during the stress, the spacial location of the intrinsic point is displaced toward the emitter which changes the location of the stress-induced interface states. This changes the value of V_G where the location of the intrinsic point (maximum recombination) coincides with the induced surface states, hence a shift of the hump.

McDonald (ref. 83) also recognized that the location of the hump is in part controlled by another phenomonon. Under large negative bias on the gate, holes are injected into the SiO_2 where they become trapped. This trapped positive charge causes a shift in the I_B versus V_G

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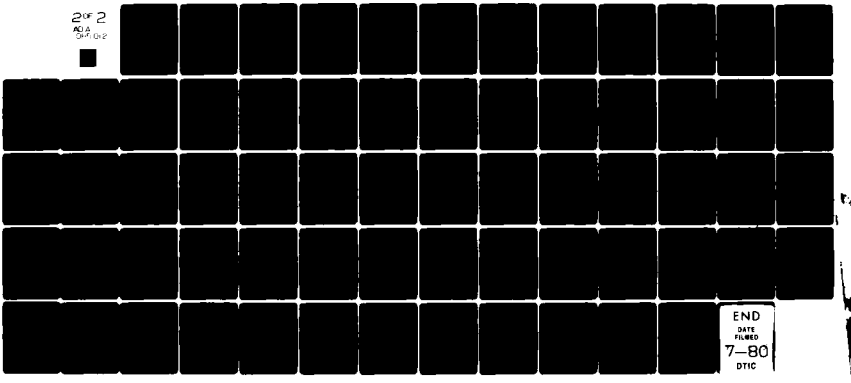

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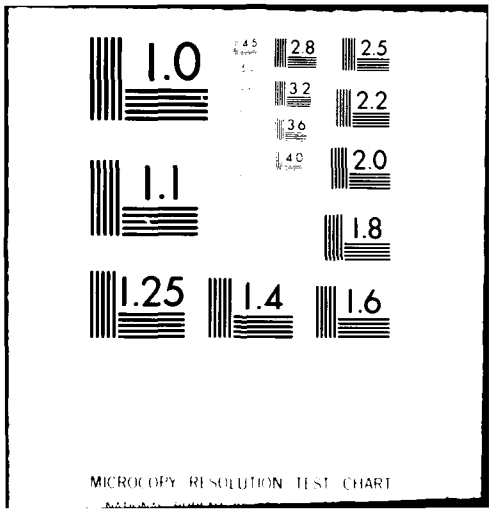
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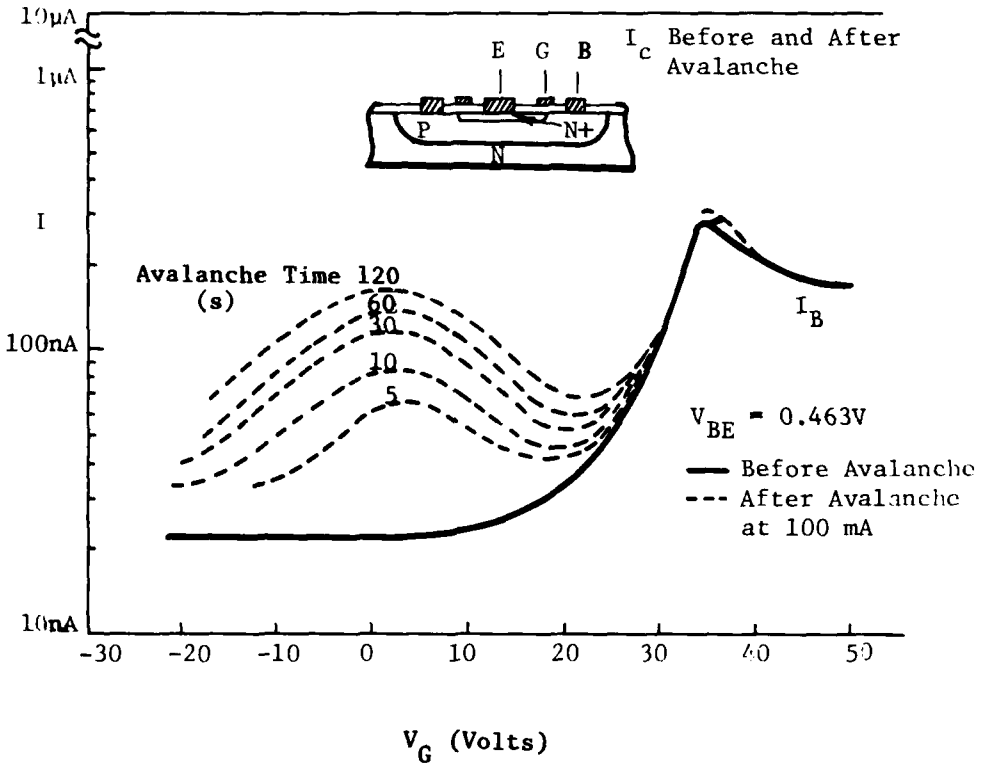

Figure 16. Effect of Emitter Avalanche on the Plot of Base Current Versus Gate Voltage for a Gate-Controlled n-p-n Transistor. Avalanching the Emitter Base Junction Causes an Additional Peak in the Plot of I_s Versus V_a and the Magnitude of this Peak Increases with Increasing Avalanche Time (Reference 83)

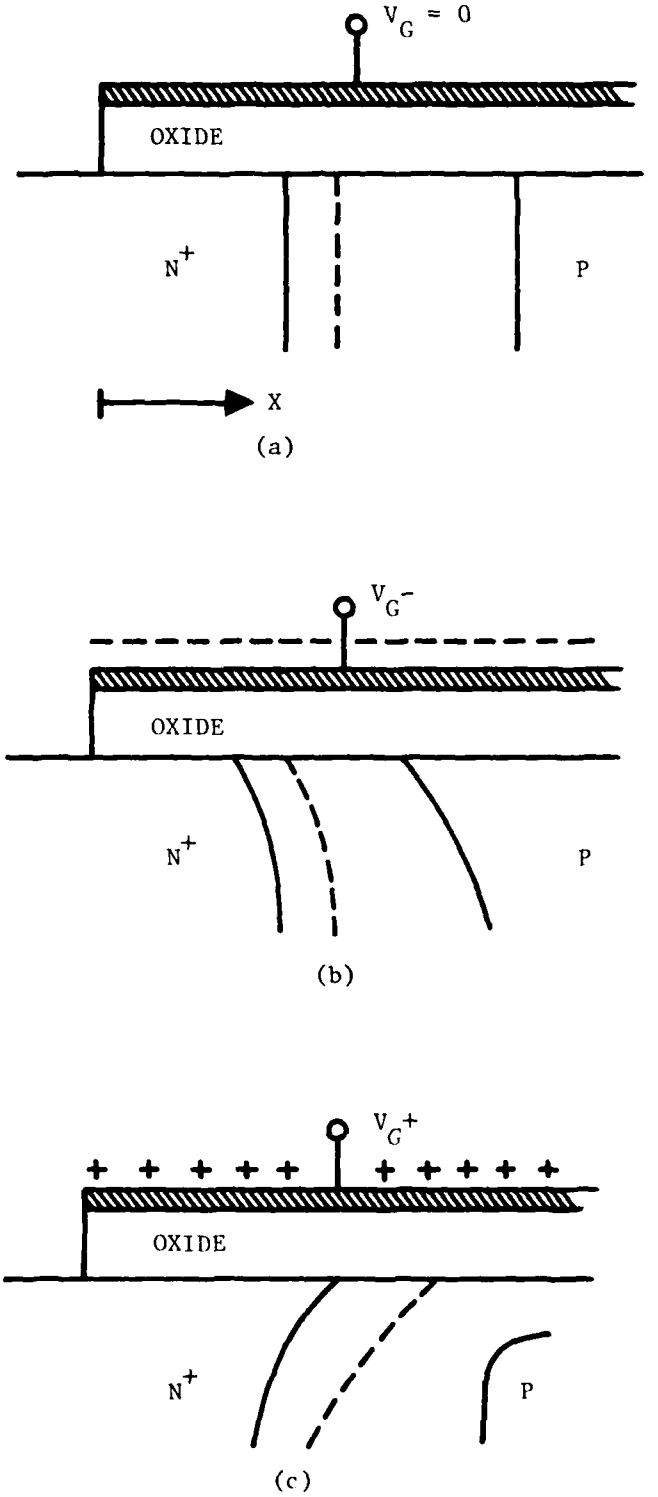

Figure 17. Effect of Gate Bias on the Intrinsic Point Within the Surface Space-Charge Layer of a Double-Diffused n-p-n Transistor. Due to the Impurity Gradient Along the Surface, the Location of the Intrinsic Point Within the Emitter Base Space-Charge Region is Surface-Potential Dependent. **(Reference 83)**

hump since negative gate voltage is required to overcome the SiO_2 positive space charge in order to bring the location of the intrinsic E-B junction back to its preirradiation value.

Verwey (refs. 84, 85) has argued that it is indeed the trapped charge in the oxide that causes a shift in the I_B peak, and the shift in the spacial location of the interface states under negative V_G stress is insignificant. Verwey argues that in npn transistors, due to boron leaching by the SiO_2, the surface region of the p base is doped lower than the bulk immediately below it. Therefore, breakdown of the E-B junction does not occur right at the surface but a distance of approximately 1 μm below the surface. This means that under positive V_G, the spacial location of the breakdown will not move appreciably into the base region. Also because of the high doping in the emitter, negative voltage on the gate will not cause appreciable depletion of the emitter, so the intrinsic point will not move very far toward the emitter. Verwey attributes the shift in the hump as due to hole trapping under negative gate bias and electron trapping under positive gate bias. This position is supported by the fact that the amount of the shift decreased toward $V_G=0$ when the devices were stored for a period of time or when the devices were irradiated with U.V. radiation. Both of these mechanisms cause an annealing of the stored charge.

Therefore, by reverse biasing an E-B junction into avalanche on a gated transistor with $V_G < 0$, both hole injection and trapping and creation of interface states can be induced. The important parameter changes resulting from this stress are shown in Figure 18 taken from Verwey (ref. 85). The preirradiation values of I_B versus V_G are shown by the solid curve. The dashed line shows the result of stressing under negative gate bias. ΔV_G^m results from hole trapping in the oxide and ΔI_B^m results from the creation of fast interface states. Under ionizing radiation, the I_B versus V_G characteristic is also altered by additional surface states and trapped positive charge. However, in the case of ionizing radiation, the trapped charge and surface states are created over a larger area of the base region, depending, of course, on the

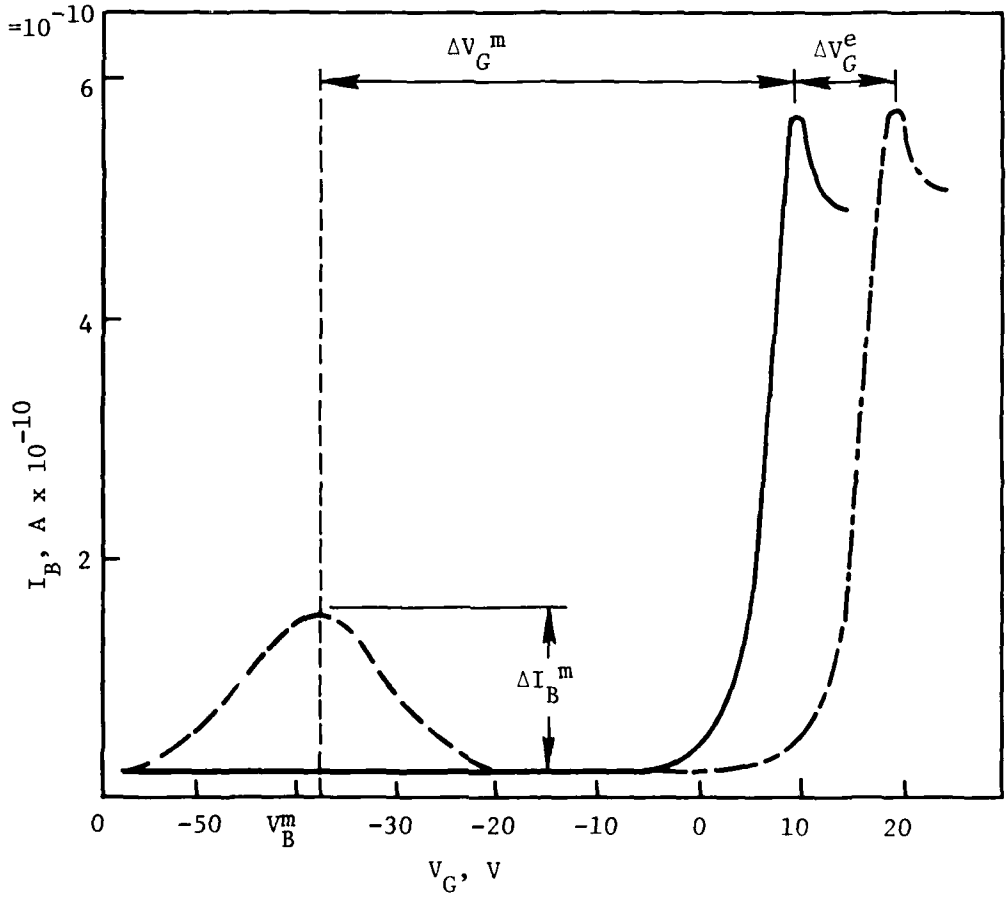

Figure 18. Base Current I_B as a function of Gate Voltage V_G at V_{BE} = 300 mV (drawn line). The Quantities ΔI_B^m, ΔV_G^m, ΔV_g^e Observable After Avalanche Breakdown (at certain gate bias see text) Are Also Indicated in the Figure. (Reference 85)

magnitude and direction of the electric field in the oxide during the irradiation. For the case of an ungated device with a large reverse V_{CB} during irradiation and V_{BE}=0, the trapped holes and surface states will be unevenly distributed along the base surface with increasing density toward the collector side of the base where the electric field is stronger during irradiation. In a gated device with a negative bias on the gate during irradiation, the trapped charge and surface states will be uniformly distributed under the gate region. Thus the distribution of induced surface states and trapped holes will be different for the E-B stress (which is highly localized) and irradiation. This can be seen by comparing the curves taken by McDonald shown in Figure 19, and Sivo's curves for a gated device irradiated with Co^{60} shown in Figure 19. The peak near V_G=0 does not appear for the irradiated device, but rather the peak which occurs at a positive V_G due to depletion of the p base is seen to increase after irradiation due to surface states and shift to the left due to trapped holes. This shift toward more negative V_G is only observed at V_{BE} = .26 volts. At V_{BE} = .5 volts, the shift is positive for reasons which are presently unknown.

Although the localization of the effects of stress results in significantly different response of I_B versus V_G curves than for radiation, there is still reason to believe a correlation will exist between ΔI_B^m from stress and $\Delta 1/h_{FE}$ from Co^{60} irradiation. If the process induced SiO_2 hole traps are fairly uniformly distributed across the base area and surface state creation results either from hole trapping, as the Svensson model suggests or holes crossing the interface as other models suggest, then for a given geometry and process, the value of ΔI_B^m and ΔV_B^m (using Verwey's notation) for a fixed stress should correlate to the radiation induced gain degradation. This hypothesis has not been verified and will require gated transistors to do so. If correlation does exist, a simple stress test on a gated device with V_G large enough to create a field of ~1MV/cm in the base oxide could serve as a simulated radiation test for bipolar circuits. The gated transistor could be located on each chip or as a separate chip located on different parts of a wafer. The stress test could be performed at the wafer level with probes.

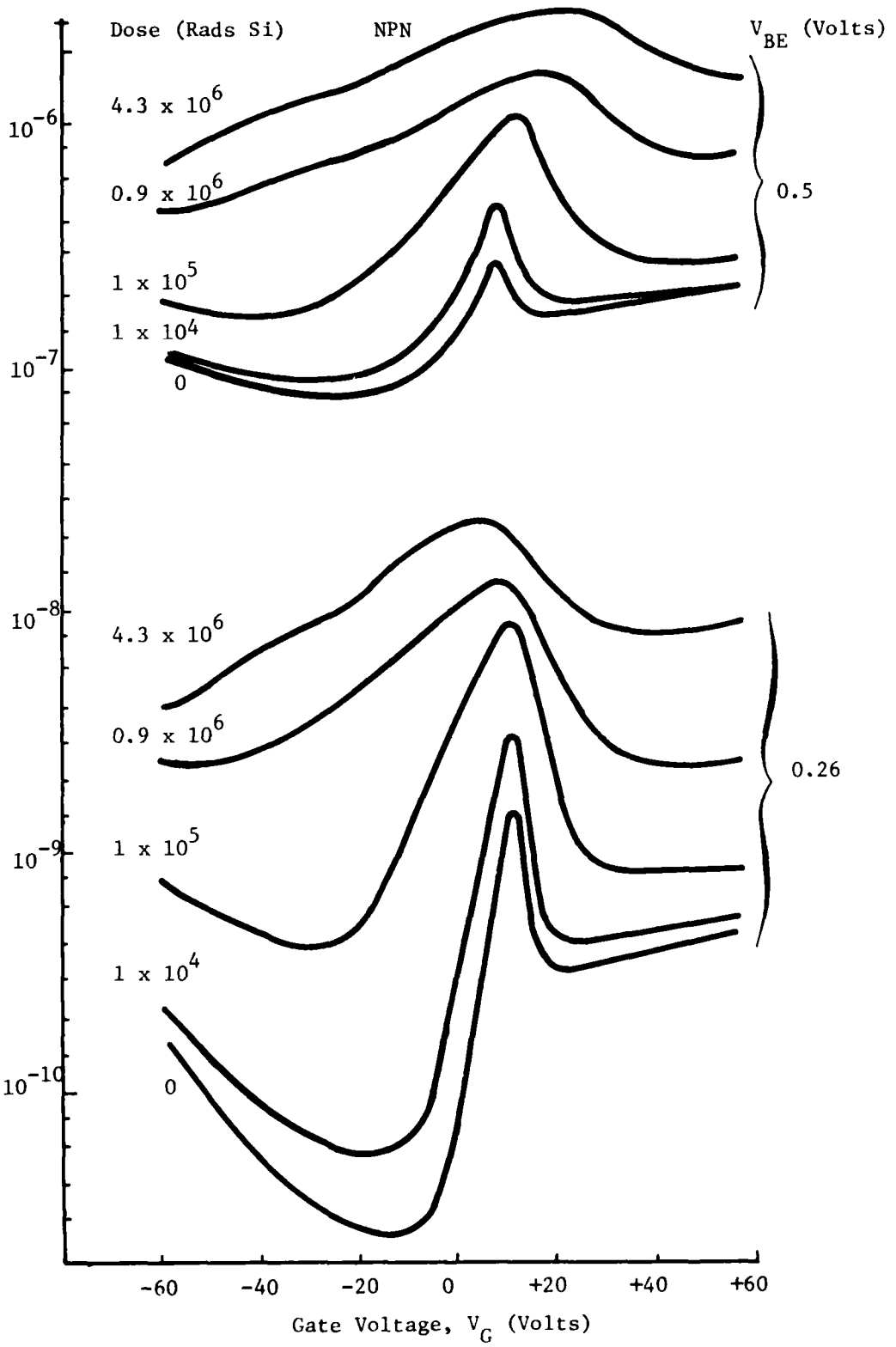

Figure 19. Effect of Ionizing Radiation on the I_B Versus V_G Curves at Various Injection Levels. Note the Increases in the Surface and Bulk (FIJ) Components of I_B as well as the Changes in the Shapes of the Current Peaks ("Broadening"). The Gain Degradation is Represented by Increases in I_B at V_G = 0. (Reference 63)

The effectiveness of such a test is unknown since no correlation tests have been run; however, if shown effective, the technique will be very practical since it can be performed with I_B versus V_G measuring equipment and a constant current source for stress. The major problem in implementation will be the requirements for a light tight probe stage and a test setup to accurately monitor currents in the 10^{-10} Amp range.

2) p-n Junction Avalanche on MOSFETS

The same techniques applied to gated bipolar transistors to study p-n junction avalanche hole injection can easily be applied to MOSFETS where the gate is an integral part of the device. Verwey (refs. 11, 12) has studied oxide hole trapping parameters by avalanching the source-substrate junction of the MOSFET with a negative bias on the gate. In order to restrict the avalanche plasma to a region near the surface, the technique is applied to n channel devices having an n+ - p junction. Since the voltage on the gate is negative the p region next to the interface is accumulated and the n+ region, because of its heavy doping, is relatively unaffected. The accumulation of the surface p region causes the breakdown to occur at the interface rather than in the bulk. Rather than measure the electrical characteristics of the MOSFET before and after stressing, Verwey measured the time dependent hole current through the oxide. From this information he extracted the product N_oS where N_o is the concentration of process-induced neutral hole traps in the oxide and S is their capture cross section.

In order to derive the product N_oS, one must first account for the fact that at a fixed gate voltage, the electric field in the oxide near the avalanche plasma changes as holes become trapped. To account for this, Verwey empirically determined the dependence of the hole current on the field from the relation

$$I_H = Ke^{\delta E}$$

where I_H is the hole current, K a proportionality constant, δ the slope of the experimental curves of I_H versus E, and E the field in the oxide. To determine the dependence of I_H on E, measurements of the peak hole current are made on separate devices of the same type with different gate voltages.

The peak current, I_t, as shown in Figure 20 from reference 12 is a measure of the hole current prior to any trapping, therefore, a plot of I_t versus E will yield δ and K for a given process.

Representative data for three wafers are shown in Figure 21. The oxide electric field in the area where holes are being injected and trapped is given by

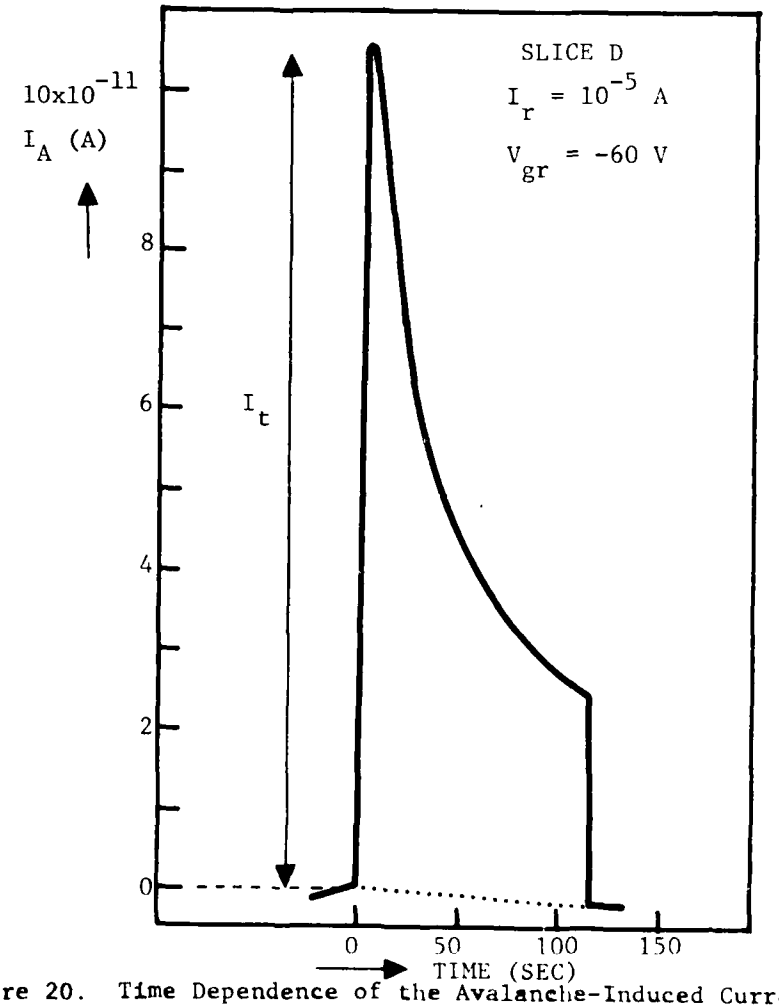

Figure 20. Time Dependence of the Avalanche-Induced Current Through the SiO_2. At t_0 a Constant Reverse Current $I_r=10^{-5}$A was Applied to the n-p Junction. The Gate Voltage was V_{gr}= -60V With Respect to the Base Region. (Reference 12)

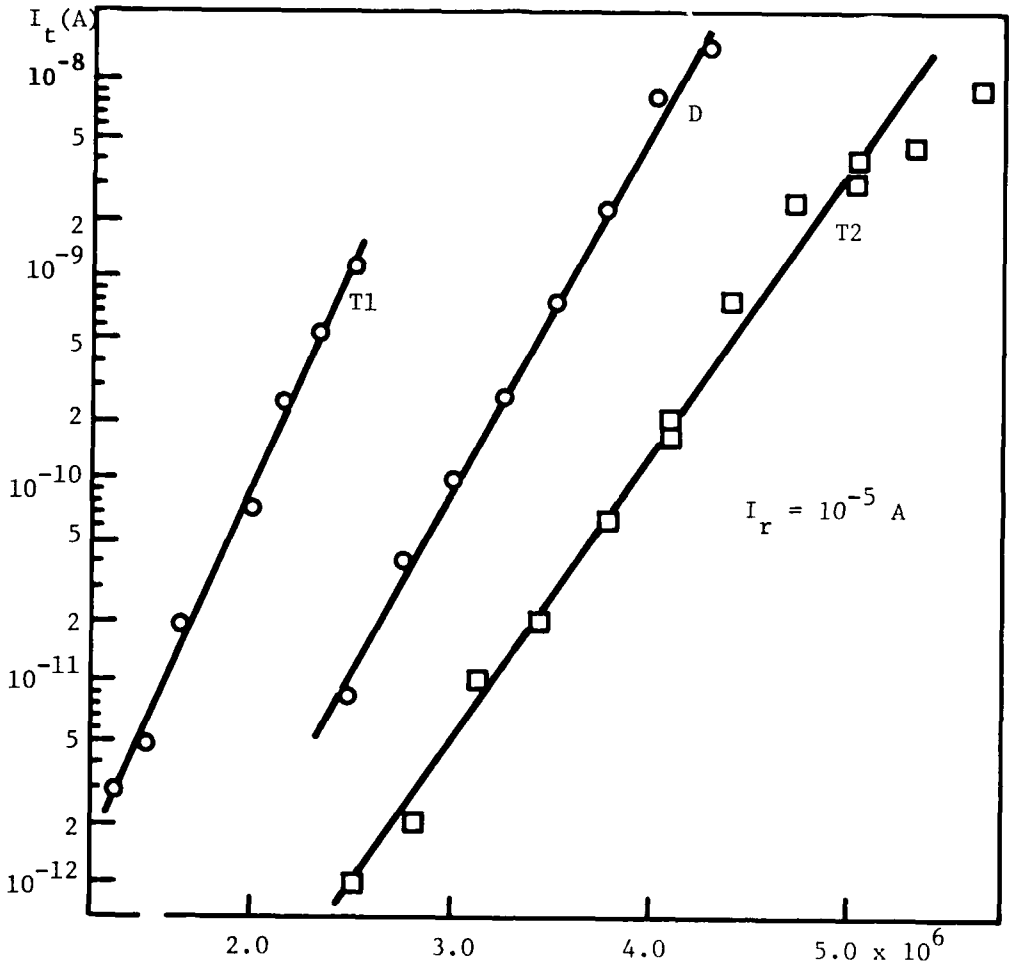

Figure 21. Dependence of I_t on the Field E in the Oxide (Reference 12)

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$$E = \frac{V_G}{t_{ox}} - q \frac{Q^+ t_{ox}}{2\varepsilon}$$

where V_G is the gate voltage, t_{ox} the oxide thickness, Q^+ the trapped positive charge and ε the oxide dielectric constant.

Using this relation and the relation between hole current, area, N_o and S, Verwey derives the equation

$$I_H = I_t \, e^{-\frac{\delta t_{ox} N_o S}{2\varepsilon A} \int I_H dt}$$

where A is the area of the avalanche plasma supplying the hole current. In order to determine $N_o S$, a plot of I_H versus $\int I_H dt$ must be generated from the I versus t curve of Figure 21. The slope, α, of the I_H versus $\int I_H dt$ curve is then given by

$$\alpha = \frac{\delta t_{ox}}{2\varepsilon A} \cdot N_o S$$

The product $N_o S$, the process induced hole trap density times its capture cross section, should be a measure of hardness. This product should then correlate with the radiation induced threshold voltage shift in those cases where ΔV_{TH} is due primarily to hole trapping.

The method used by Verwey for measuring $N_o S$ requires a lot of data acquisition and reduction. Therefore, we have considered measurements which are easier to make that might yield a hardness parameter. One possibility involves the fact that the breakdown voltage of the junction being avalanched changes as a result of charge trapping in the oxide. As more positive charge is trapped, the p region becomes less accumulated and thus the breakdown voltage increases. This increase in BV with time should indicate how quickly charge is being trapped. Thus, the rate of change of BV should be a measure of $N_o S$.

Another possibility is to maintain the junction breakdown at its initial value by adjusting the negative voltage on the gate. By increasing V_G to keep BV constant, a constant field should be maintained in the oxide. If this is done for a period long enough to essentially saturate the traps, for a given field and stress current, then the total shift in V_G required to maintain constant BV should be measure of hardness.

Still another approach would be to apply a feedback circuit between V_G and I_H to maintain a constant I_H. Once an equilbrium is reached the total change in V_G should be a measure of the total saturated value of trapped charge, hence hardness.

Although these alternative approaches may not be easier to instrument, the data reduction should be much easier.

No information was found regarding the use of MOSFET avalanche hole injection as a screen for hardness. Therefore, the effectiveness of the technique requires verification. The technique, utilizing several of the aforementioned approaches will be verified in this program.

c. Negative Bias Temperature (NBT) Stress

Another means of inducing positive charge and additional interface states in gated structures (either bipolar or MOS) is by applying a large negative field in the oxide and heating the device. The effect of negative bias stress has been investigated in several studies (refs. 17, 86).

In a recent study by Jeppson and Svensson (ref. 87), two basic mechanisms were proposed as the cause of the trapped positive charge and interface state creation. At electric fields below 6.3 MV/cm, the mechanism is diffusion controlled and is proposed by the authors as a chemical reaction at the interface involving hydrogen. The reaction given for the interface state generation and subsequent positive charge buildup is the following: interface trivalent silicon passivated with hydrogen ($\equiv Si_s$-H) reacts with the silicon dioxide ($\equiv$Si-O-Si$\equiv$) to form a surface trap ($\equiv Si_s^{\cdot}$), a trapped positive charge in the oxide near the interface ($\equiv Si_o^{+}$), a more stable hydroxyl attached to a silicon in the oxide ($\equiv$Si-OH),

and a free electron. This model accounts for both the formation of interface states and the buildup of positive charge. It is based on evidence of H at the interface and the often observed proportionality between the buildup of positive charge and the buildup of interface states. As evidence of the relation between the trapped charge Q_r and increase in interface states N_{ss}, Jeppson and Svensson present a plot of ΔV (midband), which is roughly a measure of Q_r, and the surface trap density at midband, derived from high and low frequency C-V curves. These results are reproduced here as Figure 22.

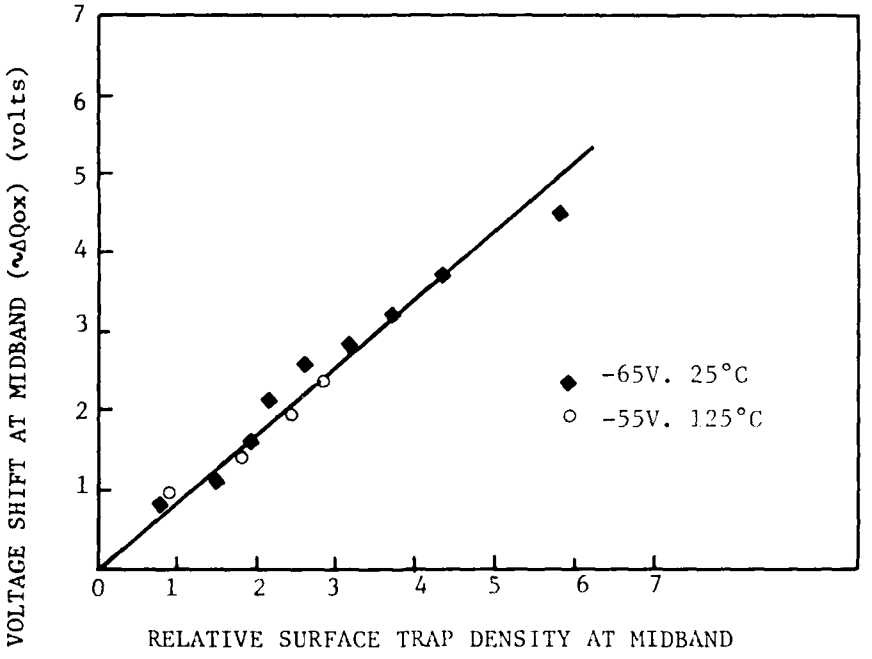

Figure 22. The increase of the oxide charge measured as the shift of the C-V curve at midband, plotted against the relative surface-trap density at midband. The same relationship is observed after NBS at both 125 °C, -55V (5.8 MV/cm) and 25 °C, -65V (6.8 MV/cm) and indicates that there is roughly one surface trap per oxide charge. **(Reference 87)**

At high negative fields in the oxide a departure from a diffusion controlled process is observed based on departure from a $(\text{time})^{1/4}$ relation for the buildup of surface traps. This transition point, which occurs at electric fields on the order of 6.3 MV/cm is attributed to tunneling of holes from the silicon into the oxide (ref. 87). This tunnelling process also gives rise to hole trapping and interface state creation and occurs much more rapidly than the diffusion controlled process.

Although several studies have been performed on the effects of negative bias temperature stress on MOS devices, the correlation between the damage caused by NBT and CO^{60} radiation has not been addressed. In order to establish that similar processes are taking place, a comparison should be made between the spacial distribution of trapped charge and the energy distribution of the interface states on identical samples subjected to the stress and radiation environments. Since this has not been done, the effectiveness of this technique cannot be established until the proper correlation studies have been performed. These will be done in the verification phase of this program.

If the technique proves to be an effective simulation of the radiation environment, it will be evaluated in phase II of this program. The NBT stress technique is practical either as a sample test at the wafer level or on packaged parts. Ideally, it would be used as a wafer level sample acceptance test. It can be implemented on any gated test device, which can be placed at various positions on the wafer or on each die. Pre- and post-stress electrical measurements can be made with probes and the stress can be performed on a heated pedestal with probes.

d. Bulk Avalanche Injection

Holes may be injected into the oxide from an n type subtrate driven into bulk avalanche. If a large negative voltage is applied to the gate of an n type MOS capacitor, it can be driven into a nonequilibrium deep depletion condition if the pulse width of the gate voltage is small compared to the minority carrier generation time.

For a large enough V_G, the electric field in the depletion region will reach the point where avalanche multiplication occurs. Some

of the minority carriers accelerated toward the $Si-SiO_2$ interface will be energetic enough to be injected into the oxide where they may be trapped by the process induced neutral hole traps.

This technique has been used by Aitken and Young (ref. 10) to study the effect of processing variations on hole trap density and by Bakowski et al. (ref. 79) to study hole trapping characteristics (e.g., spacial location and capture cross sections).

Effective use of the bulk avalanche hole injection technique requires a special MOS capacitor test structure and proper waveforms for the negative gate potential. In order to reduce the breakdown field in the bulk silicon and to minimize edge injection effects (ref. 10), a relatively high substrate doping level of $10^{17}cm^{-3}$ is required. This doping level does not often occur in either bipolar or MOS processing. The hole injection and trapping is sensitive to both gate pulse frequency and shape. Aitken and Young[8] have found that a sawtooth waveform of about 5-50 kHz works well. Bakowski et al. (ref. 79) use a constant negative voltage on which they superimpose a 1 kHz signal used to avalanche the silicon. The average current through the oxide is monitored and a feedback circuit is used to adjust the gate signal amplitude to maintain a constant current. The peak field in the oxide is maintained at 1.5-3 MV/cm.

Although Aitken and Young (ref. 10) note a similarity between the results of both positive charge trapping and interface state generation from avalanche hole injection and radiation, no detailed correlation studies were performed. The studies at JPL (ref. 79) included the use of both p and n substrate capacitors, processed at the same time. The n substrate devices, which were irradiated with Co^{60}, were then avalanched such that the injected electrons could be used to probe the radiation-induced trapped holes. From these data, the spacial distribution of the trapped holes could be determined. However, no tests were performed to verify that the effects of the hole injection and radiation were identical. In the JPL study, no significant buildup of interface states was observed.

If the bulk avalanche hole injection technique is to be utilized as a total done hardness assurance method, verification of the effectiveness of this technique as a simulation of the radiation environment must be performed. This would entail measuring the correlation between stress-induced parameter shifts (Q_r and ΔN_{ss}) and radiation-induced parameter shifts on several samples. Although the technique was given careful consideration for the evaluation phase of this program it was rejected on the basis of practicality. The requirement for a specific narrow range of doping for the n type substrate of the test MOS capacitor implies a processing variation which would be unacceptable to most semiconductor manufacturers for production devices. In addition, the test setup and volume of data required for the stressing would require a substantial development cost in order to accommodate a large volume of testing.

5. RADIATION TESTS

The only reliable and acceptable total dose hardness assurance method used to date on any known systems is a radiation test, primarily in the form of a sample test. Radiation tests fall into three main categories: (1) irradiate and anneal, (2) low dose screening, and (3) sample tests.

In a radiation test, the objective is to use a source of ionizing radiation to simulate the actual hostile environment, whether it is space radiation or ionizing radiation from a nuclear weapon. The amount of damage which occurs in a semiconductor device from total dose irradiation is proportional to the number of holes generated in the oxide and the polarity and magnitude of the electric field in the oxide. Since the energy required to produce a hole electron pair in SiO_2 is independent of the source and the total dose is measured in terms of the total energy deposited in the material (oxide), the damage should only depend on the number of rads (100 ergs/gram) deposited in the passivation layer independent of the source of the ionization. This simplification of the situation requires several assumptions:

(1) The total dose in rads(SiO_2) can be measured.

(2) The ionization is deposited uniformly in the passivation layer both for the threat environment and test environment.

(3) The ionizing radiation does not create additional hole traps or directly alter the interface structure.

(4) The energy of the ionizing radiation source is greater than the threshold for hole-electron generation in the passivation layer ($\sim$ 19 eV for SiO_2) and low enough that it does not create a significant amount of displacement damage, either in the passivation layer or the silicon.

Several ionization sources have been used to simulate the threat environment including Co^{60} and Cs^{167} gammas, various X-ray sources and electrons from linear accelerators, Van De Grafs, dynamitrons, and scanning electron microscopes (SEM's). Special care must be taken in the use of electrons from a SEM to insure that a uniform dose profile is obtained in all passivation regions of the device. Generally energies of >30 keV are sufficient when exposing an unencapsulated device.

Since the amount of hole trapping and interface state generation is a strong function of electric field in the oxide during the exposure, radiation testing should always be done under realistic worst case bias configuration.

a. Irradiate and Anneal (IRAN)

The IRAN technique is a 100 percent radiation test on the devices or circuits to be used in a system. The devices are exposed to the expected threat level dose under worst case bias conditions and any device not meeting the postradiation performance criterion is rejected. The devices passing the screen are then annealed at elevated temperature until their electrical characteristics return to within an acceptable percentage of their initial value. The devices passing this screen are then used in the system.

The IRAN technique is a rather drastic measure and generally only used when the performance of the devices is very marginal at the required dose level or the required failure rate is so low that no "maverick" behavior can be tolerated.

In order for IRAN to work well as a 100 percent screen, several criteria should be met:

(1) The hole traps in the oxide are process-induced and the radiation does not generate additional hole traps.

(2) The radiation does not directly alter the interface structure such that additional interface state generation sites are created.

(3) The thermal anneal will depopulate the trapped holes and return the interface to its initial condition.

(4) The electrical characteristics and reliability of the device will be the same at the end of the irradiate and anneal treatment as it was initially.

The validity of the technique depends on how close the real situation approximates the above criteria. The irradiate and anneal technique has been investigated in several studies (refs. 43, 45, 88, 89, 90) with mixed results.

In an early study by Nelson and Sweet (ref. 88) on 2N1613 transistors, the investigators found that a 320 °C 5-hour anneal returned the degraded electrical parameters to a value as good or slightly better than their initial value. They cycled the devices through several irradiate and anneal cycles and found good repeatability. The effect of various temperatures on the anneal of h_{FE} damage is given in Figure 23.

In a study by Poch and Holmes-Siedle (ref. 45) many transistor types were irradiated, annealed at 250 °C for 16 hours and reirradiated to the same dose (5×10^4 rad(Si)) to determine repeatability. Their results for 2N2222A's and 2N2907A's are shown in Figures 24a and 24b.

In the case of the 2N2222A's, the annealing was not complete in many cases and the devices degraded slightly more on the second irradiation. However, the two devices which degraded the most on the first irradiation repeated their behavior on the second irradiation within a few percent. The results on the 2N2907A's was rather mixed. Several showed much more degradation on the second irradiation, and at least two degraded less.

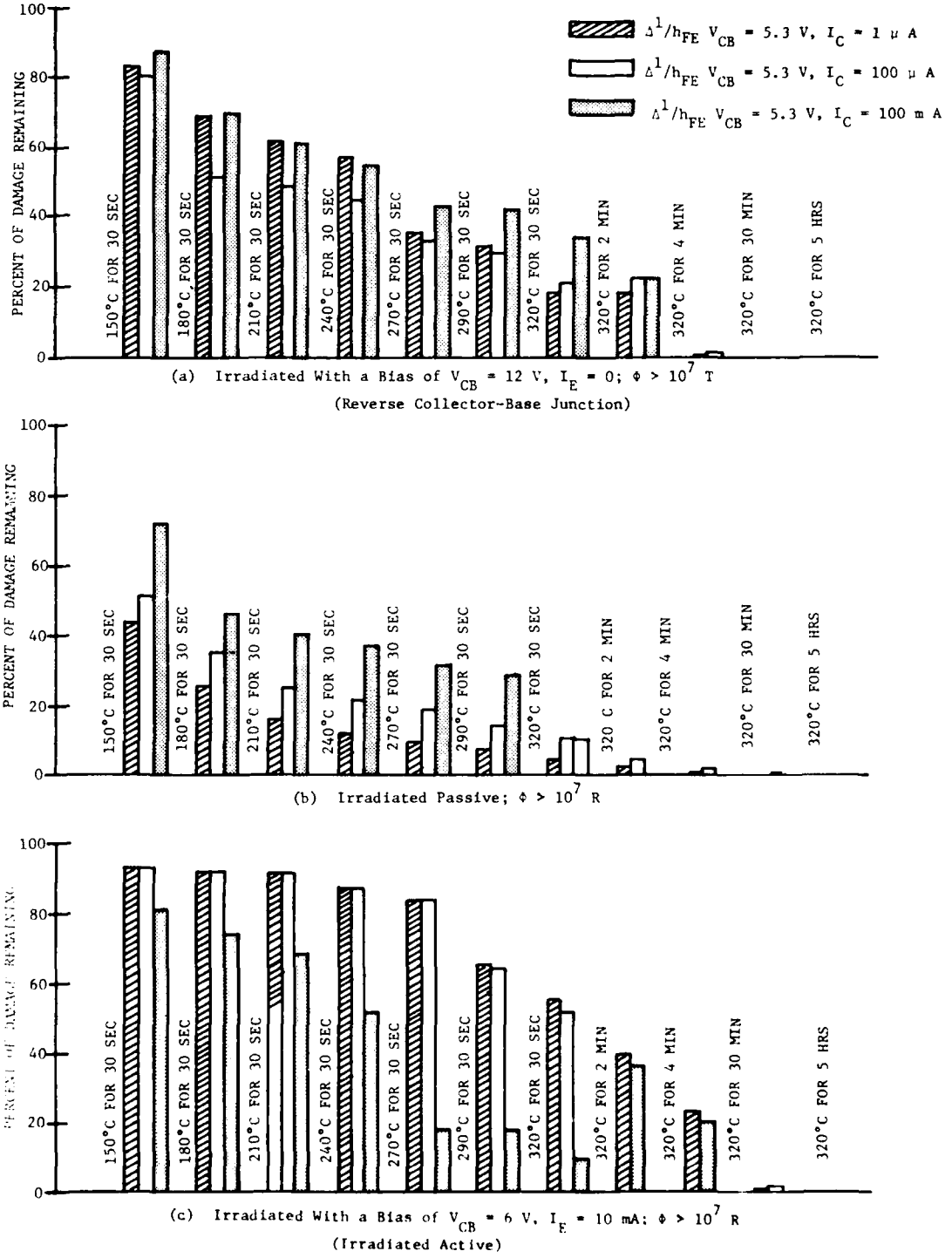

Figure 23. Effect of Temperature Stress on h_{FE} Damage Removal (Reference 88)

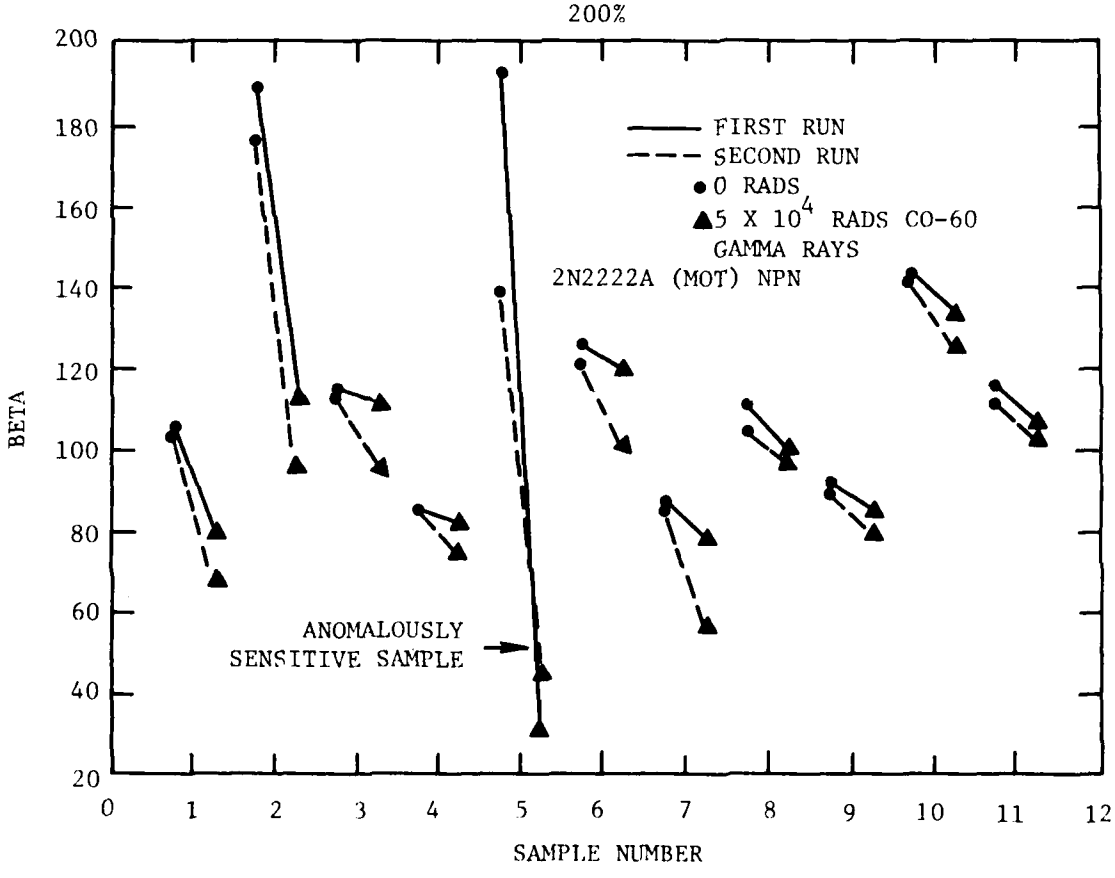

Figure 24a. Comparison of Beta Loss From Successive Irradiations of Motorola Type 2N2222A Transistor with Intermediate Annealing Step (Test Collector Current = 1 mA) **(Reference 45)**

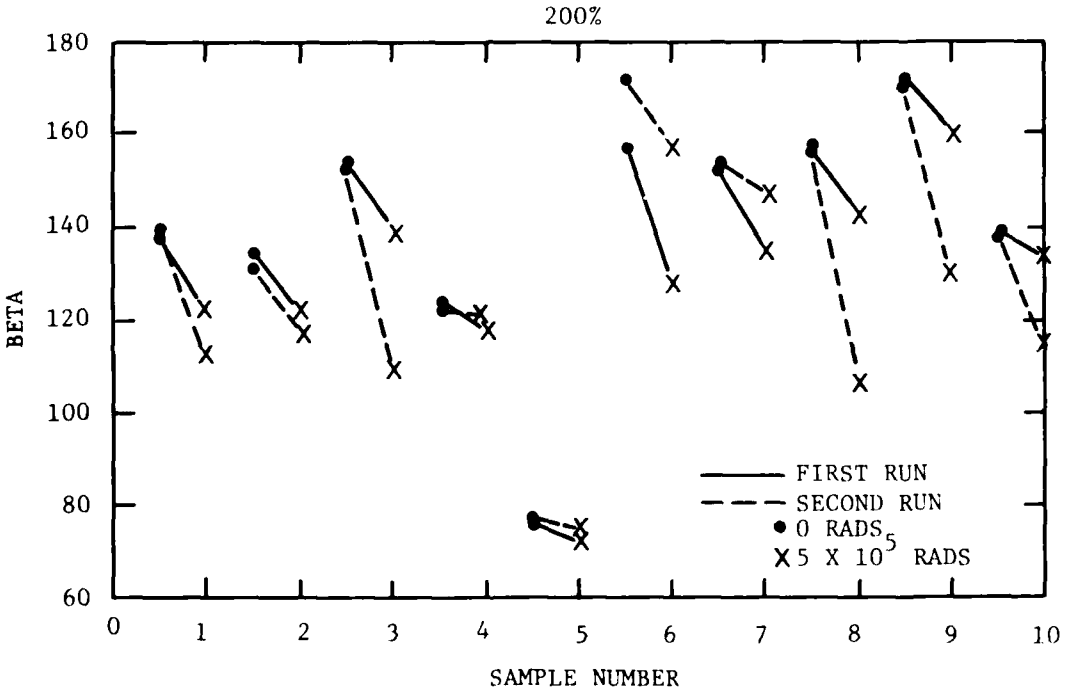

Figure 24b. Comparison of Beta Loss From Successive Irradiations of Fairchild Type 2N2907A Transistor, with Intermediate Annealing Step (Test Collector Current = 1 mA) **(Reference 45)**

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In the Boeing Study (ref. 43) the total dose irradiate and anneal was performed on a μA744 op amp and a sense amp. The irradiations were performed at three different levels and the anneals were carried out at 300 °C for 2 hours. The rank correlation between the first and second irradiations is shown in Table 9 for the μA744 and Table 10 for the sense amp at 1.3×10^6 rads.

The correlation is reasonable but does not indicate excellent retracking as might be expected especially in the case of I_{OS} on the μA744. The conclusions that Boeing reached were that for the μA744, in order to be sure that the devices would pass the requirements on the second irradiation, the margin of acceptance on the first radiation would have to be lowered by ∿20 percent. For the sense amp, the correlation between first and second irradiation was made ambiguous by the fact that the annealing was very inconsistent. They observed one device which failed during the second irradiation but not during the first. However, this part showed negative annealing and hence, would have been rejected.

The most extensive total dose irradiate and anneal program was carried out by Stanley and Price (ref. 89) for the Mariner Jupiter/Saturn spacecraft. This study included linear bipolar circuits, bipolar transistors, n-channel JFETS and analog switches. The part types considered for IRAN were characterized for repeatability before a decision was made as to whether or not to use the technique for the flight parts. The radiation levels used ranged from 50-150 Krads(Si) and all anneals were carried out at 150 °C for 96 hours. The temperature limit was imposed by the program office for reliability reasons. Such a limit severely restricts the amount of annealing that takes place and hence, for many devices, erratic results were obtained. Because of the erratic annealing and general lack of correlation between first and second irradiation, several linear circuits were rejected for flight part IRAN screens. Some general conclusions drawn from the study were:

(1) In almost all cases, reirradiation produced subtantially greater shifts than the first irradiation.

TABLE 9. RANK CORRELATION BETWEEN FIRST AND SECOND IRRADIATION PARAMETERS OF μA744 OP AMP (REFERENCE 43)

Measured Parameters	Rank Correlation Coefficient	Total Dose (rads)
V_{OS}	0.805	2.7×10^5
I_B	0.694	2.7×10^5
I_{OS}	0.588	2.7×10^5
$A_{OL}(+7.5)$	0.806	2.7×10^5
$A_{OL}(-7.5)$	0.804	2.7×10^5
V_{OS}	0.915	1.3×10^6
I_B	0.800	1.3×10^6
I_{OS}	0.709	1.3×10^6
$A_{OL}(+7.5)$	0.918	1.3×10^6
$A_{OL}(-7.5)$	0.918	1.3×10^6
V_{OS}	0.931	5.6×10^6
I_B	0.807	5.6×10^6
I_{OS}	0.702	5.6×10^6
$A_{OL}(+7.5)$	0.934	5.6×10^6
$A_{OL}(-7.5)$	0.933	5.6×10^6

TABLE 10. RANK CORRELATION BETWEEN PARAMETERS OF THE SENSE AMP MEASURED AFTER 1.3×10^6 Rads DURING THE FIRST AND SECOND IRRADIATION CYCLE (REFERENCE 43)

Measured Parameters		Rank Correlation
I_{OS}	CH 1	0.952
I_B	CH 1	0.950
V_{OS}	CH 1	0.960
A_{OL}	CH 1	0.960
I_{OS}	CH 2	0.900
I_B	CH 2	0.898
V_{OS}	CH 2	0.905
A_{OL}	CH 2	0.931
I_{OS}	CH 3	0.876
I_B	CH 3	0.883
V_{OS}	CH 3	0.880
A_{OL}	CH 3	0.860
I_{OS}	CH 4	0.926
I_B	CH 4	0.923
V_{OS}	CH 4	0.925
A_{OL}	CH 4	0.920

(2) The 150 °C anneal brought most parameters back to within the manufacturer's specification limits even if the annealing was not complete.

(3) The response of most linears was a slow parameter change up to 3.5×10^4 rads, then a logarithmic increase. For the second irradiation, the logarithmic increase started at about 1×10^4 rads.

(4) Most of the anomalies could be eliminated by a suitable acceptance criterion applied to the first irradiation data but which was specific to each parameter of each device.

In general, the technique was found to have limited usefulness especially for linear circuits and with the limitation of a 150 °C anneal.

The repeatability of radiation damage in MOSFETS was studied by Danchenko (ref. 90) et al. in a paper on thermal annealing characteristics. The study involved p channel enhancement mode devices irradiated to 5×10^{12} e/cm^2 (E_e = 1.5 MeV). The repeatability of six IRAN cycles on six devices is shown in Figure 25. These devices were annealed at 300 °C for 2 hours. It is clear in this case that repeated IRAN cycles improved the hardness of these devices, with the shift becoming slightly smaller with each cycle.

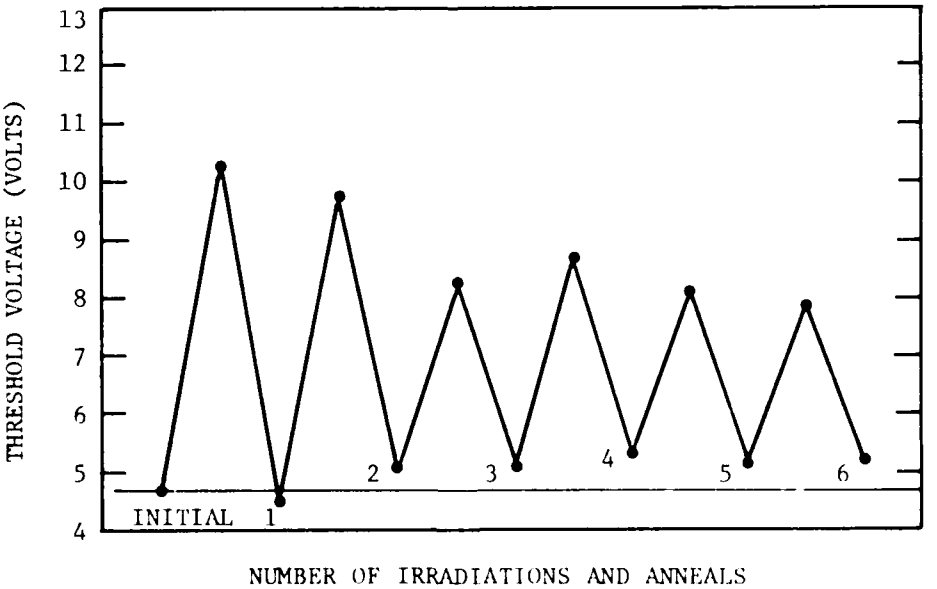

Figure 25. Changes in the Threshold Potential as a Function of the Radiation-Annealing Cycles. Upper and Lower Points are Irradiations and Anneals, Respectively. (Reference 90)

The effectiveness of IRAN is somewhat in question. From the data presented in the studies cited, it appears that temperatures of 300 °C or greater are necessary for proper annealing. It also appears that linear bipolar circuits are not very repeatable even with a 300 °C anneal. In order for the anneal to work effectively, all devices should be stabilized at the anneal temperature for several hours before the first irradiation is performed. It is not clear whether or not this was done in all cases. Most data on annealing of trapped holes indicate that temperatures of 250-300 °C are sufficient. However no definitive data were found on the annealing of interface states generated from radiation. Derbenwick* found that on irradiated MOS capacitors the 1 MHz C-V curve, which showed severe stretchout indicating surface states, translated toward its initial value without changing slope for anneal temperatures up to 250 °C. Above 250 °C, the distortion disappeared indicating an annealing of interface states.

The lack of annealing of interface states could explain the erratic results of the JPL study due to the temperature limit on the anneal.

In order for the effectiveness of IRAN to be established, additional studies on the annealing characteristics of interface states, and a determination of whether or not radiation produces additional hole traps should be made.

IRAN is a practical technique, in terms of its implementation, since it involves the same process used in sample testing. However, it is very expensive. Part of the cost involved in IRAN could be saved if it could be performed at the wafer level. No previous studies of wafer level IRAN have been found since no way has been devised to provide bias to every circuit on the wafer during irradiation. It has been suggested that a SEM equipped with wafer probes could be used. However, with this technique, each chip would have to be individually scanned by the SEM while the bias was being applied through the probes. The time and expense of this approach would be prohibitive.

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*NOTE: Private communication with Gary Derbenwick.

A method for wafer level IRAN, under bias, using Co^{60} as the radiation source has been suggested by Tausch of BDM*. This method involves the use of a special interdigitated metallization pattern that would run along the scribe lines at the edge of each chip. All leads to be grounded would be brought to a common point at the edge of the wafer and connected to a large bonding pad. The leads to be biased would be brought to a common point opposite the ground leads. The wafers would be mounted in a special fixture equipped with probes for irradiation in a Co^{60} source.

If the original metallization pattern were designed to include the irradiation bias interconnects, then only one additional step would have to be included in the process. After the metal pattern is laid down and the wafers irradiated, that portion of the metallization used for chip interconnects would be etched off before wafer probe. The post-radiation acceptance limits would then be used for the go-no-go probe data. All circuits which fail postradiation would be inked out and rejected. The wafer would then go through an additional sinter step at 400-500 °C to anneal out the damage before being packaged. As suggested by Ports of Harris Semiconductor, a fuse in the form of a metallization neckdown can be added to each circuit in the bias interconnect so that reject circuits drawing excessive current will be removed from the bias. If such provisions were not made, proper bias could not be established during irradiation.

The advantages of doing wafer level IRAN are:

(1) Radiation failures are rejected before expensive packaging and final test.

(2) No additional electrical tests have to be performed. Acceptance is based on dc wafer probe.

(3) Annealing of radiation damage can be performed at a higher temperature without affecting reliability since it is performed at the wafer level.

Possible shortcomings of the technique are:

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*NOTE: Private communication with Jake Tausch.

(1) Special metal pattern required.

(2) Additional processing step required.

(3) Excessive wafer handling is necessary to perform Co^{60} irradiation.

(4) Effects of packaging on radiation performance are not determined. This could be handled by a special sample test for each package type.

b. Low Dose Screening

In the low dose screening technique, all devices are exposed to a total dose level much lower than the expected threat level and devices exhibiting unacceptable parameter shifts are rejected. The screen dose level is chosen so that only the marginal and reject devices show a measureable change in parameters. Since the parameter shifts on acceptable devices are so small, no annealing is required. Hence the method is like IRAN without the anneal. In order for low dose screening to work properly, the parameter shifts at low dose levels must correlate with the parameter shifts at the specification dose level so that the relative degradation for a given sample with respect to others in the lot remains constant with dose.

The effectiveness of low dose screening has been evaluated for bipolar transistors (ref. 45) and op amps (ref. 43). Poch and Holme-Siedle (ref. 45) reported that the anomalously sensitive 2N2222A devices tested at 5×10^4 rads were also the most sensitive devices at 230 rads. Thus they suggest that a screen at 100-1000 rads would identify "maverick" devices without causing a measureable change in good devices. They note, however, that R. R. Brown of Boeing observed devices which did not degrade anomalously at low doses and did show excessive degradation at a high dose.

Arimura et al. (ref. 43) report that low dose screening is totally ineffective for op amps.

Although low dose screening is an attractive technique, due to the elimination of the annealing step, it must be rejected as a viable method due to its ineffectiveness.

c. Sample Radiation Tests

It is generally conceded within the hardness assurance community that the only acceptable total dose screen is a sample radiation test, under bias, on packaged devices. This idea was expressed at a workshop on total dose hardness assurance held at BDM Albuquerque (17 July 1978) which was attended by 30 people active in total dose basic mechanisms studies and hardness assurance. This generally accepted idea is stated in the first draft of the "Total Dose Irradiation Effects Guidelines," (written by Stanley, Martin, Price, and Gauthier of JPL for The Defense Nuclear Agency) as follows: "There are no reliable correlations of pre-irradiation electrical parameter values to the post-irradiation performance of a semiconductor device in a total dose radiation environment. For this reason the main reliance must be placed on radiation quality conformance tests...."

Presently, a radiation sample test is the only hardness assurance technique considered effective. However, there are many ways to implement a radiation sample test. In this program, radiation sample tests will be evaluated to determine the following:

(1) What statistics best apply to the distribution of radiation-induced parameter shifts?

(2) How large are the wafer-to-wafer and lot-to-lot variations in response?

(3) How good is the correlation between circuit failure and selected device failure?

The statistics of total dose response has been studied in detail by Stanley, Martin, and Price (ref. 91). They observe a log normal distribution of radiation induced parameter shifts for bipolar transistors and op amps. Using log normal statistics, they have developed sampling plans, data reduction schemes, and acceptance criteria. This contrasts with the acceptance criteria used for other quality conformance tests based on normal distributions.

Wafer-to-wafer, lot-to-lot, and process-to-process variations in total dose response have been studied in numerous programs. As may be

expected, most of these studies have concluded that the largest variations occur from process-to-process followed by lot-to-lot variations. Wafer-to-wafer variations are generally smaller but may still be significant. Thus, the sampling plan must include samples from every wafer if total dose failure levels are close to the specification level. If the margin between specification dose and nominal failure level is quite large, then lot sampling is acceptable.

6. SUMMARY AND CONCLUSIONS

The identification phase of this program has involved three approaches for identifying viable total dose hardness assurance techniques. The first approach was to search all of the available literature on total dose testing, hardening, and hardness assurance to determine what techniques have been tried or suggested. The second approach was to study the basic mechanisms of total dose effects in semiconductors and review all of the proposed models for radiation-induced hole trapping and interface state generation. An exercise was then carried out whereby possible tests, either direct or indirect, were conceived which could be used to verify the model. These tests would then serve as total dose screens if the model were verified. For example, if the process induced neutral hole traps are assumed to be due to trivalent or excess silicon near the SiO_2-Si interface, then a measure of the density of these centers using, for instance, ESR, should serve as a screen for the effects of hole trapping.

The third approach was to consider known sensitive process parameters which affect the total dose hardness. Knowing the sensitive processing steps, potential techniques were considered which could be used to determine the process parameters. For the most part this cannot be done by the user on the fabricated device. Therefore, the only way to assure that certain processes are adhered to is to place controls on the manufacturer during processing. This approach is difficult to implement.

Once all of the possible hardness assurance techniques, either identified in the literature or conceived from a model, were identified, they were evaluated for effectiveness and practicality. The effectiveness of any hardness assurance technique must ultimately be based on empirical data. Therefore, all available data taken for a particular technique were reviewed to determine how well the predictive parameter correlated to the total dose radiation response. For the most part, data were either lacking or ambiguous. Thus, if the effectiveness of the technique was in question but it was considered practical, the technique was subjected to verification testing to determine its effectiveness. Those techniques considered impractical were dropped from further consideration. The practicality of each technique was evaluated on the basis of cost, impact on processing, and potential impact on reliability. The most important factor, cost, includes the capital equipment required, the amount of labor for both data acquisition and data reduction, and effect on yield. The determination of the practicality of a technique is somewhat subjective, since it involves the willingness of a user to pay for the test or control and the willingness of the manufacturer to implement the technique. What a customer is willing to pay for is dependent on his total budget and what portion he is willing to spend on hardness assurance. Thus, what is practical to a strategic or satellite system may be totally impractical for a tactical system. Also, what one manufacturer may be willing to accept may be totally out of the question for another manufacturer. Thus, the only techniques which were rejected on the basis of practicality were those which were obviously cost prohibitive when compared to full scale radiation tests.

Although it was desired that all practical techniques whose effectiveness was in question would be verified by empirical tests, this proved difficult for some methods. Those techniques which require special test structures not available commercially or in-process testings, such as would be performed on pilot wafers, were not included in the verification testing. Since there were several techniques that could not be properly verified in the first phase of the program, the evaluation phase was

restructured to allow for preliminary verification testing before full scale evaluation is performed. Any technique proven ineffective in the verification testing will be dropped from further consideration.

A summary of the total dose hardness assurance techniques identified in this program are given in Table 11 along with our assessment of their effectiveness and practicality. Those techniques to be verified in phase I of this program are identified, along with the techniques that will have to be verified in phase II. Techniques which are considered both effective and practical are indicated as being acceptable for full scale evaluation. Also included in Table 11 are the test structures required and technologies and devices types to which the technique applies.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES

TECHNIQUE

Bipolar Transistor Preirradiation Electrical Parameters.

EFFECTIVENESS

No correlation has been established between bipolar, transistor total dose response and any preirradiation electrical parameter including h_{FEO}, I_{BO}, I_{EBO}, 1/f noise, BV_{EBO}, I_B (ΔT), ΔI_B (burn-in) and characteristic of BV_{EBO} curve.

PRACTICALITY

COST FACTORS: Minimal
Only cost of extra testing

PROCESS IMPLICATIONS: None

APPLICABILITY

TECHNOLOGY: Bipolar
DEVICE TYPES: Transistors

IMPLEMENTATION

TEST STRUCTURES: None

REQUIRED TESTS: Preirradiation electrical

OVERALL ASSESSMENT

Reject - Ineffective

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Input Transistor Operating Current, I_1, on Bipolar Linear Circuits.

EFFECTIVENESS

Proved effective as a processing lot screen on several lots of AMD LM108As. Has not been verified on any other devies.

PRACTICALITY

COST FACTORS: Requires special electrical test on external pins.

PROCESS IMPLICATIONS: None

APPLICABILITY

TECHNOLOGY: Bipolar

DEVICE TYPES: Linear circuits for which I_1 can be measured.

IMPLEMENTATION

TEST STRUCTURES: No special.

REQUIRED TESTS: 100 percent I_1 test.

OVERALL ASSESSMENT

Very limited technique requires verification on every circuit to which it will be applied. Verify in phase I.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Total Charge In Oxide Using a-c conductance or noise measurements.

EFFECTIVENESS

According to Nicollian and Goetzberger the total charge in the oxide is related to the standard deviation of the frequency response of the a-c conductance of a MOS capacitor and to the stand deviation of the range over which the noise follows a 1/f dependence. These predictions are based on the random potential fluctuations caused by the charge near the interface. No tests have been performed to assess this relation.

PRACTICALITY

COST FACTORS: Requires special test device.
Would require extensive test circuit design and software in order to automate for either a-c conductance or noise measurements.

PROCESS IMPLICATIONS: Mask design change to incorporate test capacitor.

APPLICABILITY

Limited to hole trapping screen.

TECHNOLOGY: A

DEVICE TYPES: Any

IMPLEMENTATION

TEST STRUCTURES: MOS capacitor.

REQUIARED TESTS: a-c conductance versus f at fixed gate bias or noise versus f at fixed gate bias.

OVERALL ASSESSMENT

Applicability limited.
Effectiveness not determined.
Could involve high initial cost to automate date aquisition and analysis.
Verification required for dipole model and relation between total charge and measured quantities. Verify phase I.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Charge Localization from low temperature substrate bias affect.

EFFECTIVENESS

Michael Pepper has menonstrated that the change in condustivity at low carrier concentrations on p channel MOSFETS measured at 4.2 °K changes less as a function of substrate bias on "hard" oxides than it does on "soft" oxides. The effectiveness of this measurment as a screen for hardness has only been assessed on two sets of specially fabricated MOSFETS.

PRACTICALITY

COST FACTORS: Requires cryogenic equipment and liquid helium source. Requires hand measurements.

PROCESS IMPLICATIONS: None

APPLICABILITY

Only measure of hole trapping.

TECHNOLOGY: Any

DEVICE TYPES: Any

IMPLEMENTATION

TEST STRUCTURES: MOS FET.

REQUIRED TESTS: Channel conductance versus gate voltage with and without substrate bias at 4.2 °K.

OVERALL ASSESSMENT

Effectiveness only partially verified impractical because of equipment requirements. Reject for this program .

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Imputity Content In Oxide As Prediction Of Trapped Holes.

EFFECTIVENESS

H. Hughes et al found correlation between sodium content in oxide and hardness. However, the sodium concentrations were much high than encountered in standard devices. No correlations has been found between mobile positive charge and hardness. G. Hughes showed that devices on a wafer with high impurity content (many different impurities) was softer than a wafer with low impurity content. No definitive tests have been performed to correlate pre rad oxide impurity content with hardness for a large sample with a reasonable range of impurity content.

PRACTICALITY

COST FACTORS: Would require spectroscopic analyzer to measure impurity content. Should be sensitive down to $10^{10}/cm^2$ on a 1000 Å oxide.

PROCESS IMPLICATIONS: Would probably require a test or pilot. Wafer for each oxide being investigated.

APPLICABILITY

trapped holes.

TECHNOLOGY: Any

DEVICE TYPES: Any

IMPLEMENTATION

TEST STRUCTURES: Test wafters.

REQUIRED TESTS: Measure impurity content of oxide on test wafer.

OVERALL ASSESSMENT

Cannot be used as 100 percent device screen or wafer level screen. Has not been verified for effectiveness on commercial or military parts. Reject impractical and too limited.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Hand/or OH content at interface as screen for radiation induced interface states.

EFFECTIVENESS

Most models of interface state generation involve hydrogen incorporated in some manner at the interface as typing up dangling bonds and thus inactivating a defect center. On radiation and hole trapping the hydrogen is released leaving a dangling bond and hence an interface state. No one has correlated the concentration of hydrogen at the interface with radiation induced buildup of N_{ss}. However, evidance of this relation is sighted for the difference in ΔN_{ss} for wet and dry oxides.

PRACTICALITY

COST FACTORS: Only know method of measuring H or OH at interface is internal reflection spectroscopy in the infrared. This is a highly specialized experimental setup.

PROCESS IMPLICATIONS: Requires special test wafers.

APPLICABILITY

Can only be used as wafer lot screen for ΔN_{ss}

TECHNOLOGY: Any

DEVICE TYPES: Any

IMPLEMENTATION

TEST STRUCTURES: Test wafers

REQUIRED TESTS: Must measure H and/or OH conent at interface on special test wafer using infrared internal reflection spectroscopy.

OVERALL ASSESSMENT

Technique is too limited in applicability and is impractical for production monitoring. Also effectiveness has not been determined.

Reject for this program.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Initial value of N_{ss} (midgap) as measure of ΔN_{ss} from radiation.

EFFECTIVENESS

If the number of dangling bonds at the interface pasified by hydrogen is high then the number of radiation induced interface states should be high according to a generally accepted model of ΔN_{ss}. An indirect measure of the amount of initial passivation is the surface recombination velocity using a gated diode. In the hydrogen passivation model is sufficient, then there should be an inverse correlation between N_{ss} (initial) and ΔN_{ss}. No definitive data was identified which investigated the relation between N_{ss} and ΔN_{ss} (λ). Data by Sivo indicates

PRACTICALITY

COST FACTORS: Minimal - measurements can be made at D.C. probe however data must be recorded and reduced.

PROCESS IMPLICATIONS: Requires design of specail test strucure.

APPLICABILITY

Limited to prediction of ΔN_{ss} (λ) at wafer or chip level.

TECHNOLOGY: Any

DEVICE TYPES: Any

IMPLEMENTATION

TEST STRUCTURES: Special gated diode with on-chip electro meter (MOSFET)

REQUIRED TESTS: D.C. voltage proporational to I_R measured at three or more gate biases.

OVERALL ASSESSMENT

Test structure could be placed on every chip or in a pattern on each wafer. Method is practical using special gated diode structure. Effectiveness has not been determined.

Verify in Phase II.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Measurement of dipole density from initial interface state density at bond edges.

EFFECTIVENESS

Pepper claims hole traps in oxide are related to dipole density near interface. Dipoles may cause bond tailing which results in edge states. Therefore preirradiation edge states may correlate to hole trap density. No experimental data has been taken that investigates correlation between edge states and depole density or radiation induced hole trapping.

PRACTICALITY

All known direct measurments of edge states involve liquid nitrogen temperature.

COST FACTORS: Cryrogenic equipment required.
Hand recorded data and involved data reduction.

PROCESS IMPLICATIONS: Requires test capcitor.

APPLICABILITY

Only measure of hole trapping.

TECHNOLOGY: All

DEVICE TYPES: All

IMPLEMENTATION

TEST STRUCTURES: Requires an MOS capacitor on both n and p type substrates.

REQUIRED TESTS: Any direct technique for measuring N_{ss} at E_c and E_V.

OVERALL ASSESSMENT

Effectiveness not verified. No practical measurement of edge states is known. Reject because impractical.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Change in interface stress due to viscons oxide flow as a prediction of hole trap density.

EFFECTIVENESS

The viscons shear flow model of hole trapping attributes the hole traps in the SiO_2 to microscopic viscons flow of the oxide at elevated temperatures. Therefore, a measure of the change in stress at the interface during oxidation cool down and subsequent high temperature processing is a measure of hole trap density. EerMise has taken preliminary data that supports this hypothesis.

PRACTICALITY

COST FACTORS: Would require specially built and calibrated equipment for monitoring the change in stress on a test wafer in situations during high temperature operations.

Hand measurements and data reduction.

PROCESS IMPLICATIONS: In-process monitoring of stress on test wafer. No process engineer would allow it.

APPLICABILITY

Only used as wafer lot screen for trapped holes.

TECHNOLOGY: All

DEVICE TYPES: All

IMPLEMENTATION

TEST STRUCTURES: Test wafer

REQUIRED TESTS: Stress measurement in situ after oxidation and again at end of processing.

OVERALL ASSESSMENT

Effectiveness not well established. Not practical. Reject for this program.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Q_{ss} measured after oxidation but before annealing.

EFFECTIVENESS

In the model of Maier, based on the excess silicon model, a complex mathematical formula is derived in which the hole trap density is related to oxide growth temperature and pressure, Q_{ss} and N_{ss}. The formula predicts that the hole trap density is proportional to the rate of growth which in turn is proportional to Q_{ss} measured after oxidation, before annealing. This hypothesis has not been experimentally tested.

PRACTICALITY

COST FACTORS: Minimal

PROCESS IMPLICATIONS: Requires measurements on test wafers.

APPLICABILITY

Only good as wafer lot screen for trapped holes.

TECHNOLOGY: All

DEVICE TYPES: All

IMPLEMENTATION

TEST STRUCTURES: Special test wafers with capacitor metallization layed down immediately after the critical oxidation step.

REQUIRED TESTS: Must measure high frequency C-V curves at 300½C with first positive then negative gate bias. This determines mobile charge which must be substrated out to get Q_{ss}.

OVERALL ASSESSMENT

Based on model. No experimental data. Limited applicability. Verify in Phase II.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Monitor oxide thickness as an indicator of total dose hardness.

EFFECTIVENESS

The dependence of the MOS capacitor flatband voltage shift on oxide thickness is a well established fact. There is however, some disagreement as to the actual functional dependence for a uniform irradiation. Derbenwick and other invertigators have found a t_{ox}^3 relation for thin oxides (<1000Å) whereas G. Hughes has found a t_{ox}^2 dependence for thicker bipolar oxides. In addition to use as hardness control, t_{ox} is an excellent process control monitor since it is strongly affected by oxidation temperature, ambient, and crystall orientation.

PRACTICALITY

COST FACTORS: Minimal

Requires an ellipsometer which most semiconductor manufacturers have.

More of cost impact on bipolar where t_{ox} is not generally monitored as carefully.

PROCESS IMPLICATIONS: Need spcial test wafer for each critical oxide

APPLICABILITY

TECHNOLOGY: All

DEVICE TYPES: All

IMPLEMENTATION

TEST STRUCTURES: Test wafers

REQUIRED TESTS: Accurate determination of t_{ox} for each critical oxide using ellipsometer.

OVERALL ASSESSMENT

No verification required.

t_{ox} is excellent process control monitor but limited as a hardness predictor. For a fixed process, hardness goes as t_{ox}^n (where $2<n<3$). However, in this case t_{ox} does no vary appreciably across a wafer, wafer to wafer or lot to lot. In comparing different processes the hardness varies with many parameters and t_{ox} many be a second order effect.

Evaluate in phase II is process control monitor.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Silicon surface defect density as a predictor of hardness.

EFFECTIVENESS

A considerable amount of experimental data has been taken to establish the relation between the silicon surface defect density (as revealed by a chemical etch) and hardness. Both the initial surface defect density and the processed induced defect density have been investigated. There is disagreement on how well the defect density predicts hardness and whether initial or process induced defects are more important. There is also some dispute over which types of defects are important and what is the best etch to reveal them. However, the data taken on MOS gate oxides indicates that within a given lot, devices having a larger defect density will be softer. No quantitative realtion between #defects/cm^2 and ΔV_{FB} has been established and verified over several process lots.

PRACTICALITY

COST FACTORS: Requires extra test wafers and chemical etching. Requires manual counting of etch pits over small area of wafer.

PROCESS IMPLICATIONS: Minimal

Requires additional device quality wafers.

APPLICABILITY

Wafer level screen

TECHNOLOGY: MOS - has not been shown effective for bipolar.

DEVICE TYPES: All

IMPLEMENTATION

TEST STRUCTURES: Test wafers.

REQUIRED TESTS: As process control a sample of the as received device quality wafers should be etched and counted. If # defects/cm^2 is above an acceptable limit, then surface should be etched in HO vapor at 1200°C until ~10um is removed. As hardness indicator a test wafer or portion of device wafer which has gone thru processing should be etched and counted.

OVERALL ASSESSMENT

May be usefull as relative indicator of MOS gate hardness within a processing lot. Will not be included for evaluation in this program.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Process controls for total dose hardness assurance.

EFFECTIVENESS

Several detailed investigations of the affect of various processing steps on total dose hardness have identified all of the major variables. Based on these results proper processing procedures have been established especially for MOS gate oxides. Major factors which affect hardness (other than impurities, surface defects and t_{ox} which were treated separately) are crystal orientation, oxidation temperature, oxidation ambient, anneal ambient, anneal temperature, metallization system and sintering temperature and ambient . Control of these factors has been demonstrated to be an effective means of achieving hardness.

PRACTICALITY

Factors mentioned above must be controlled by manufacturer during processing.

COST FACTORS: Additional training and documentation.
Additional cleaning procedure.
Additional monitoring equipment.

PROCESS IMPLICATIONS: All details of processing must be controlled and frequently monitored.

APPLICABILITY

TECHNOLOGY: Any

DEVICE TYPES: Any

IMPLEMENTATION

TEST STRUCTURES:

REQUIRED TESTS: Frequent calibration of monitoring equipment. Frequent tests for purity of chemicals. Test for precision of crystall orientation.

OVERALL ASSESSMENT

The process controls mentioned above can be implemented by the manufacturer to assure hard devices. However, they cannot be monitored by the user on test devices or the finished product. Therefore, from the standpoint of a program office or user they are not useful screens.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Corona discharge, as simulation of radiation effects.

EFFECTIVENESS

G. Hughes has shown correlation between ΔV_{FB} (corona) and ΔV_{FB} (Co^{60} on six wafers. Still some uncertainty about basic physical process involved in the hole trapping and interface state generation from negative corona discharge.

PRACTICALITY

COST FACTORS: Requires special non commerical experimental setup to produce corona.
Need special test capacitor for measuring ΔV_{FB}.

PROCESS IMPLICATIONS: Special test wafer.

APPLICABILITY

Wafer lot screen.

TECHNOLOGY: Any

DEVICE TYPES: Any

IMPLEMENTATION

TEST STRUCTURES: Special test wafer for each critical oxide.

REQUIRED TESTS: Test wafer is charged by negative corona for $\sim$ 1 minute. ΔV_{FB} is measured using special test capacitors.

OVERALL ASSESSMENT

Effectiveness has been verified on small sample. Technique requires highly speciallized test equipment and procedures. Considered impractical for production testing compared to radiation test. Reject for this program.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

p-n Junction Avalance Hole Injection as Simulation of Radiation Effect.

EFFECTIVENESS

On both commercial bipolar transistors and specially designed gated transistors, several investigators have shown that low current h_{FE} can be severly degraded by avalanching the E-B junction, especially with a negative electric field in the oxide. Verwey has measured the field and time dependence of the oxide hole current in MOSFETS under negative gate bias and source-subtrate or drain-subtrate breakdown. No data has been identified in which the correlation between avalanche injection degradation and radiation induced degradation has been determined.

PRACTICALITY

COST FACTORS: Wafer probe station with necessary stress circuit and device parameter measurement circuit if used as wafer level screen.

PROCESS IMPLICATIONS: For bipolar it would require design of special test transistors with gate over E-B junction.
For MOS it would require n channel MOSFET.

APPLICABILITY

Sample wafer level screen - destructive
TECHNOLOGY: All
DEVICE TYPES: Can be used on packaged n channel MOSFETS for other devices it requires special test device.

IMPLEMENTATION

TEST STRUCTURES: Gated bipolar transistor
n-channel MOSFET

REQUIRED TESTS: Optimum test parameters have not been determined.

Potential test are:
Bipolar - stress device and measure $\Delta 1/h_{FE}$
MOS - determine $\langle N_t \sigma \rangle$ using Verwey technique discussed in text.

OVERALL ASSESSMENT

Effectiveness not determined. Requires verification. Appears to be a practical wafer level sample test screen. Verify in Phase I.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Negative Bias Temperature (NBT) stress as Simulation of Radition Effects.

EFFECTIVENESS

The generation of interface states and buildup of positive oxide charge from NBT stress at temperatures between 25°C-300°C and fields of 1-7 MeV/cm have been investigated in several studies. Jeppson and Svensson have obserbed two mechanisms for the increase in N_{ss} and positive charge buildup which occur at different field strength. No tests results were found in which the correlation between NBT stress degradation and radiation induced degradation were determined.

PRACTICALITY

COST FACTORS: Minimal
Requires sample tests at 300°C
under bias.
If done at wafer level requires probe station
with heated pedestal.

PROCESS IMPLICATIONS: Requires test device except for MOSFET lines.

APPLICABILITY

Wafer level screen - destructive
TECHNOLOGY: All
DEVICE TYPES: Used directly on MOSFETS special test device
for other device types.

IMPLEMENTATION

TEST STRUCTURES: MOSFET or MOS capacitor.

REQUIRED TESTS: Test devices stressed with negative gate bias at 300°C. V_{FB} or V_{TH} monitored before and after to determine change due to stress.

OVERALL ASSESSMENT

Effectiveness not determined.
Appears to be a practical wafer level sample test.
Verification will be performed in Phase I.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Bulk Avalanche Injection as simulation of Radiation Effects.

EFFECTIVENESS

The effects of processing variables on the generation of neutral hole traps in the oxide have been investigated by IBM and JPL using bulk avalanche injection of holes on MOScapacitors. Both have indicated a simularity in the hole trapping process between avalanche injection and radiation. However, neither have thoroughly investigated the correlation between ΔV_{FB} (avalanche) and ΔV_{FB} (Co^{60}) for a reasonable sample.

PRACTICALITY

COST FACTORS: Requires special circuitry for maintaining constant hole current in oxide during avalanche.

PROCESS IMPLICATIONS: Requires an MOS test capacitor with n type substrate doping in a narrow range around $10^{17}/cm^3$. Proper substrates doe not occur in most process. Therefore, an implant may be required.

APPLICABILITY

Sample wafer level test.

TECHNOLOGY: All

DEVICE TYPES: All

IMPLEMENTATION

TEST STRUCTURES: MOS capacitor on n substrate doped to $\sim 10^{17}/cm^3$ for all critical oxides.

REQUIRED TESTS: Apply specified negative gate voltage waveform to create bulk avalanche and hole injection. Voltage amplitude adjusted to maintain constant hole current. Monitor V_{FB} before and after stress to obtain ΔV_{FB}.

OVERALL ASSESSMENT

Effectiveness not determined on large scale.

Practicality limited by substrate doping requirements.

Verify in Phase II.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Irradiate and Annel (IRAN) on Packaged Devices.

EFFECTIVENESS

IRAN has been investigated in several studies with mixed results. However, if the anneal time and temperature is sufficient (300½C for 2-6 hours) to restore the device to its preirradiation condition then IRAN seems to work as a 100 percent screen.

PRACTICALITY

COST FACTORS: Every device must be irradiated in a suitable ionizing radiation source under bias.
All critical electrical parameters must be monitored 100 percent before and after radiation.
All devices have to be annealed and remeasured to assure proper annealing.

PROCESS IMPLICATIONS: None

APPLICABILITY

TECHNOLOGY: All

DEVICE TYPES: All

IMPLEMENTATION

TEST STRUCTURES: None

REQUIRED TESTS: 100 percent electrical (critical parameters) pre, post rad, post anneal.
100 percent irradiation under bias.
100 percent annealing.

OVERALL ASSESSMENT

Has not been evaluated on large scale under proper annealing conditions.

Practicality is limited by cost of 100 percent radiatin testing. Evaluate in Phase II.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Irradiate and Anneal (IRAN) at Wafer Level.

EFFECTIVENESS

This approach has never been investigated. The effectiveness of IRAN appears good on packaged parts when anneal properly. The difference between this technique and IRAN on packaged parts is the effect on hardness due to die bonding sealing and the package itself. No thorough investigation of packaging effects on radiation response have been performed. However, it is known that some packaging techniques degrade hardness.

PRACTICALITY

COST FACTORS: 100 percent wafer level irradiations.
Redesign of metal mask.

PROCESS IMPLICATIONS: Metallization mask must include bias network to all circuits with fuses. Extra mask required for removal of bias metallization after radiation. Wafer handling must be well controlled.

APPLICABILITY

TECHNOLOGY: All

DEVICE TYPES: All

IMPLEMENTATION

TEST STRUCTURES: None
Does require special metal mask.

REQUIRED TESTS: 100 percent irradiation of wafers.
Limits on post rad D.C. probe must reflect post rad requirements.

OVERALL ASSESSMENT

Wafer level IRAN can save unnecessary packaging.

Anneal can be performed at 300-400½C before packaging without affecting reliability. Effectiveness not determined.

Practicality limited by extra processing. Verify in Phase II.

TABLE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Continued)

TECHNIQUE

Low Dose Screening.

EFFECTIVENESS

At least one study has shown that the relative positions of the amount of degradation for a group of devices (even from the same process) does not remain fixed as a function of dose. A device which appears to be reasonably hard at a low dose level may degrade excessively at a higher dose.

PRACTICALITY

COST FACTORS: Same as IRAN but without anneal.

PROCESS IMPLICATIONS: None

APPLICABILITY

TECHNOLOGY: All

DEVICE TYPES: All

IMPLEMENTATION

TEST STRUCTURES: None

REQUIRED TESTS: Same as IRAN but without the anneal.

OVERALL ASSESSMENT

Not effective - reject.

TABE 11. SUMMARY OF HARDNESS ASSURANCE TECHNIQUES (Concluded)

TECHNOLOGY

Sample Radiation Tests.

EFFECTIVENESS

Only presently accepted technique known to be effective.

PRACTICALITY

COST FACTORS: Requires sample radiation test under bias.

PROCESS IMPLICATIONS: None

APPLICABILITY

TECHNOLOGY: All

DEVICE TYPES: All

IMPLEMENTATION

TEST STRUCTURES: None

REQUIRED TESTS: Pre and post rad electrical on test samples.
Radiation test under bias.

OVERALL ASSESSMENT

Proven technique.

In this program the statistical distribution of response will be investigated along with wafer to wafer and lot to lot variations. Also the correlation between device failure and circuit failure will bee studied. Evaluate in Phase II.

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DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Kaman Sciences Corp.
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ATTN: P. Jessen
ATTN: M. Bell

Litton Systems, Inc.
ATTN: G. Maddox
ATTN: J. Retzler

Lockheed Missiles & Space Co., Inc.
ATTN: J. Smith
ATTN: J. Crowley

Lockheed Missiles & Space Co., Inc.
ATTN: M. Smith
ATTN: C. Thompson
ATTN: P. Bene
ATTN: E. Smith
ATTN: H. Phillips
ATTN: E. Hessee

M.I.T. Lincoln Lab.
ATTN: P. McKenzie

Magnavox Govt. & Indus. Electronics Co.
ATTN: W. Richeson

Martin Marietta Corp.
ATTN: W. Brockett
ATTN: H. Cates
ATTN: W. Janocko
ATTN: R. Gaynor

Martin Marietta Corp.
ATTN: E. Carter

McDonnell Douglas Corp.
ATTN: M. Stitch
ATTN: Library
ATTN: D. Dohm

McDonnell Douglas Corp.
ATTN: D. Fitzgerald
ATTN: J. Holmgrem

McDonnell Douglas Corp.
ATTN: Technical Library

Mission Research Corp.
ATTN: C. Longmire

Mission Research Corp.
ATTN: R. Pease

Mission Research Corporation—San Diego
ATTN: J. Azarewicz
ATTN: R. Berger
ATTN: J. Raymond
ATTN: V. Van Lint

Mitre Corp.
ATTN: M. Fitzgerald

Motorola, Inc.
ATTN: A. Christensen

Motorola, Inc.
ATTN: L. Clark

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

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National Semiconductor Corp.
ATTN: R. Wang
ATTN: A. London

University of New Mexico
ATTN: H. Southward

Northrop Corp.
ATTN: P. Eisenberg
ATTN: J. Srour
ATTN: T. Jackson

Northrop Corp.
ATTN: D. Strobel
ATTN: P. Gardner
ATTN: L. Apodaca

Physics International Co.
ATTN: Division 6000
ATTN: J. Huntington
ATTN: J. Shea

R & D Associates
ATTN: R. Poll
ATTN: C. MacDonald
ATTN: S. Rogers

Rand Corp.
ATTN: C. Crain

Ratheon Co.
ATTN: J. Ciccio

Ratheon Co.
ATTN: H. Flescher
ATTN: A. Van Doren

RCA Corp.
ATTN: V. Mancino
ATTN: G. Brucker

RCA Corp.
ATTN: D. O'Connor
ATTN: Office N103

RCA Corp.
ATTN: R Killion

RCA Corp.
ATTN: E. Van Keuren
ATTN: J. Saultz

RCA Corp.
ATTN: W. Allen

Rensselaer Polytechnic Institute
ATTN: R. Gutmann

Research Triangle Institute
ATTN: Sec. Office for M. Simons, Jr.

Rockwell International Corp.
ATTN: T. Oki
ATTN: V. Strahan
ATTN: V. De Martino
ATTN: G. Messenger
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DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Rockwell International Corp.
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Rockwell International Corp.
ATTN: T. Yates
ATTN: TIC BA08

Sanders Associates, Inc.
ATTN: L. Brodeur

Science Applications, Inc.
ATTN: V. Verbinski
ATTN: J. Naber
ATTN: V. Ophan
ATTN: D. Long

Science Applications, Inc.
ATTN: W. Chadsey

Science Applications, Inc.
ATTN: D. Stribling

Singer Co.
ATTN: J. Brinkman

Singer Co.
ATTN: R. Spiegel

Solar Energy Research Institute
ATTN: A. Stanley

Sperry Rand Corp.
ATTN: Engineering Laboratory

Sperry Rand Corp.
ATTN: C. Craig
ATTN: P. Maraffino
ATTN: F. Scaravaglione
ATTN: R. Viola

Sperry Rand Corp.
ATTN: D. Schow

Sperry Univac
ATTN: J. Inda

Spire Corp.
ATTN: R. Little

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

SRI International
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ATTN: A. Whitson
ATTN: P. Dolan

Systron-Donner Corp.
ATTN: J. Indelicato

Teledyne Ryan Aeronautical
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Texas Instruments, Inc.
ATTN: A. Peletier
ATTN: R. Stehlin

Texas Instruments, Inc.
ATTN: F. Poblenz

TRW Defense & Space Sys. Group
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ATTN: A. Pavelko
ATTN: A. Witteles
ATTN: P. Guilfcyle
ATTN: O. Adams
ATTN: H. Holloway

TRW Defense & Space Sys. Group
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ATTN: R. Kitter
ATTN: M. Gorman

TRW Systems and Energy
ATTN: G. Spehar
ATTN: B. Gilliland
ATTN: D. Millward

Vought Corp.
ATTN: Library
ATTN: Technical Data Center
ATTN: R. Tomme

Westinghouse Electric Co.
ATTN: L. McPherson

Westinghouse Electric Corp.
ATTN: H. Kalapaca
ATTN: D. Crichi